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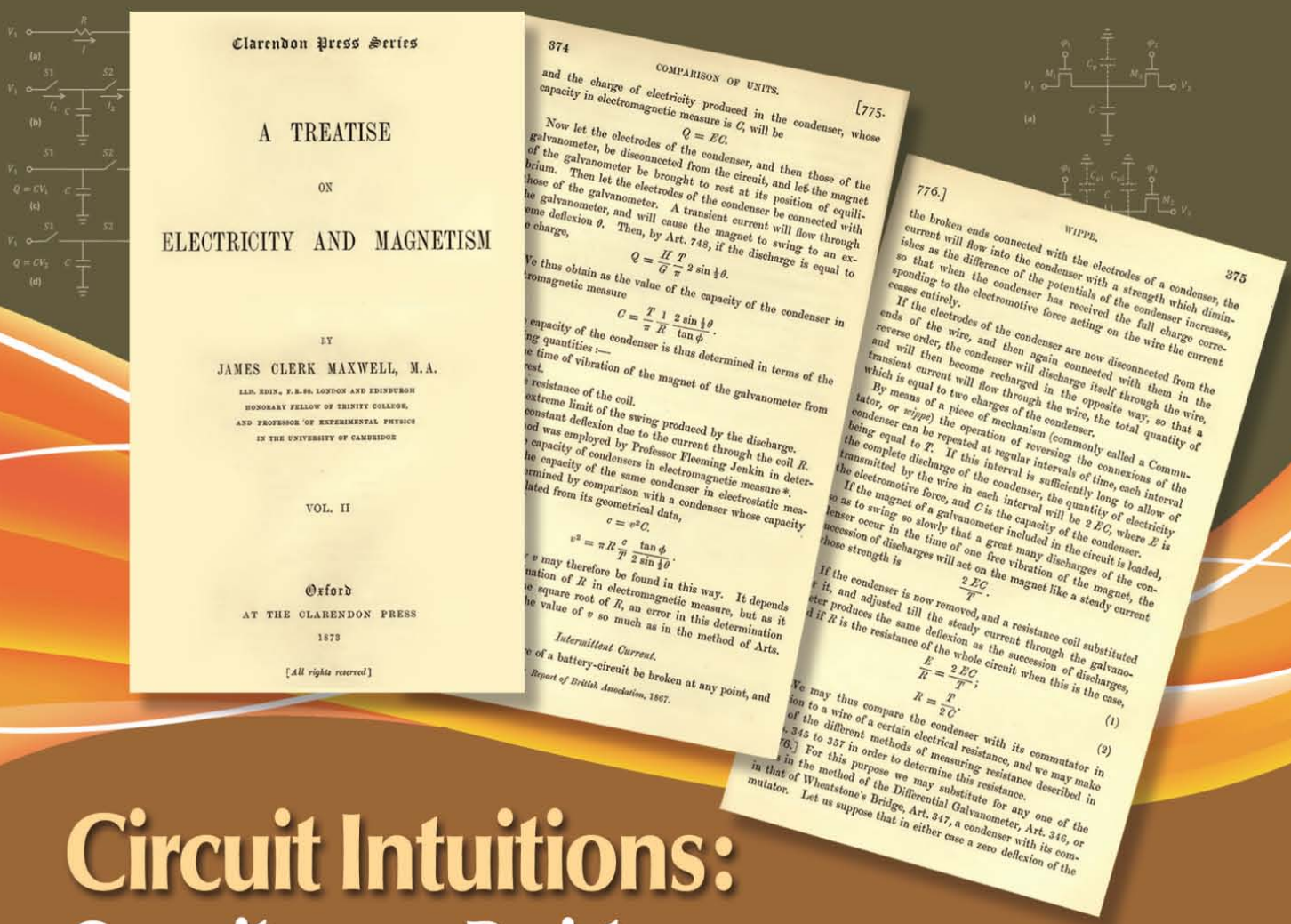

Circuit Intuitions:

Capacitor as a Resistor (Switched-Capacitors) as Taught by James Clerk Maxwell

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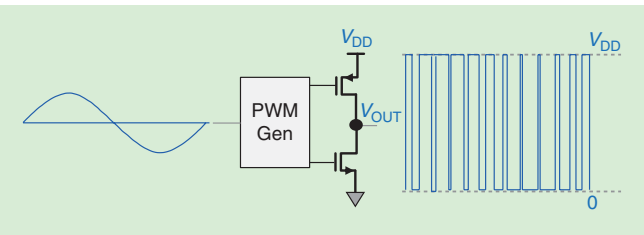
FEATURES



ABOUT THIS IMAGE:
Read "Fundamentals of Audio Class D Amplifier Design" to learn more about this amplifier.

COLUMNS/DEPARTMENTS

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SCOPE: Each issue of *IEEE Solid-State Circuits Magazine* is envisioned as a self-contained resource for fundamental theories and practical advances within the field of integrated circuits (ICs). Written at a tutorial level and in a narrative style, the magazine features articles by leaders from industry, academia and government explaining historical milestones, current trends and future developments.

CONTACT INFORMATION: See the "Contact Us" page on SSCS Web site: http://ewh.ieee.org/soc/sscs/index.php?option=com_content&task=view&id= 10&Itemid=3.

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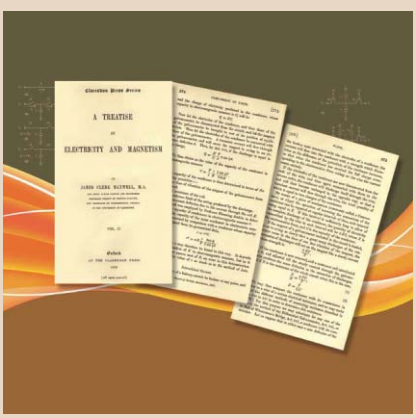

BACKGROUND—IMAGE LICENSED BY INGRAM PUBLISHING

ABOUT THE COVER:
The "Circuits Intuition" column discusses capacitors as resistors, a concept first explained by James Clerk Maxwell in his book, A Treatise on Electricity and Magnetism.

EDITOR'S NOTE

R. Jacob Baker

Welcome to the Summer 2017 Issue of *IEEE Solid-State Circuits Magazine*!

In this third issue of the ninth year of *IEEE Solid-State Circuits Magazine*, we are pleased to publish feature articles of interest to the magazine's readers ranging from tutorials to technology overviews. These include the always well-received columns from Marcel Pelgrom, Ali Sheikholeslami, and Behzad Razavi. Marcel's always entertaining article this month is "Back to Basics" and provides an engineer's view of various aspects of life. Ali's consistently informative "Circuit Intuitions" column discusses the "Capacitor as a Resistor" and is the inspiration behind this issue's cover. Behzad's article, about the flash analog-to-digial converter (ADC), provides both an excellent introduction and tutorial to one of the most useful ADC topologies.

In addition, we have the following feature articles in this issue of interest to our readers:

- "Fundamentals of Audio Class D Amplifier Design," by Xicheng Jiang
- "Nanoscale MOSFET Modeling," by Christian Enz, Francesco Chicco, and Alessandro Pezzotta
- "To EVM or Two EVMs?" by Marco Vigilante, Earl McCune, and Patrick Reynaert.

Ali's always informative "Circuit Intuitions" column discusses the "Capacitor as a Resistor" and is the inspiration behind this issue's cover.

The goal of the magazine continues to be to provide Society news and information as well as a series of self-contained resources to keep the IEEE Solid-State Circuits Society member up to date with changes in technology while, at the same time, providing reviews of circuit design concepts. This includes contributions from experts describing the current state of affairs and evolution of a particular IC technology. We will also continue to feature articles focused on the contributions of luminaries. Of course, suggestions from readers are always welcome.

We hope you enjoy reading *IEEE Solid-State Circuits Magazine*. Please send your comments to me at rjacobbaker@gmail.com

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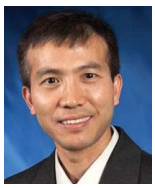
CONTRIBUTORS



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PRESIDENT'S CORNER

Jan Van der Spiegel

Summer Reflections

I write this column as I am returning from the IEEE Custom Integrated Circuits Conference (CICC) in Austin, Texas. The conference was a great success with more than 300 people in attendance. With a wide array of technical sessions, a riveting plenary session, and networking, the meeting was the perfect blend. I'd like to congratulate the members of the Organizing and Technical Program Committees for putting together a first-rate conference. You can read more about the event in the "Conference Reports" column in this issue.

One of the highlights of CICC was a very successful Young Professionals (YP) Mentoring Event held by IEEE Solid-State Circuits Society (SSCS) YP Chair Emre Ayranci. Our YP program has now evolved into a high-end mentoring event. At the YP Mentoring Event at CICC, we had two prestigious luminaries from Silicon Labs speak at the event and provide the future generation of the Society with solid advice that they can carry with them as they move forward in their lives and careers. Afterward, other Senior Members and SSCS leaders offered their advice, and a productive networking event ensued. You can read about this event in the "Society News" column of this issue.

We also filmed a series of videos at CICC called CICCx Circuit Insights. These will be short 10-min videos on the topics that were covered at the conference. The videos will be posted on our newly launched SSCS Resource Center (resourcecenter.sscs.ieee.org). The SSCS Resource Center is a hub of educational content. You can find past webinars, tutorials, short courses, and open-access papers on the site. Please keep your eyes open for the launch of the CICCx videos.

I am pleased to report that the SSCS is continuing to have a strong year of membership growth, service, and activity.

As I reflect back on the midpoint of my second year of presidency, I am pleased to report that the SSCS is continuing to have a strong year of membership growth, service, and activity. We have made great strides in setting forth a number of new initiatives and benefits. These include the following:

- In Education, we had multiple design contests for both students and professionals, the production of online courses such as CICCx, and the continuation of the growth of our widely popular SSCS Webinar and Distinguished Lecturer Programs.
- In Membership, programs include the development of the SSCS mobile app to engage our future workforce and a series of planned membership campaigns. One of these include a senior membership campaign. I encourage you to apply to become an IEEE Senior Member if you are eligible. Details are outlined on the SSCS website: http://sscs.ieee.org/membership/become-a-senior-member.
- In Publications, the Society will be launching a new publication called *SSCS-Letters*, a fast-paced publication of original contributions emphasizing transistor-level design of integrated circuits. The planned launch for this publication is early 2018.

We are tracking to be a landmark year in 2017. We will continue to deliver on the promise of our mission and excellence, focused by our strategic plan, to provide membership service with dedication and efforts to support the Society, while continuing to build a strong future for our members.

As always, please feel free to contact me with your ideas and comments at president-sscs@ieee.org.

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ASSOCIATE EDITOR'S VIEW

Marcel Pelgrom

Back to Basics

The first thing that struck me was the extreme neatness inside the school building. With it being in Switzerland, I should not be surprised. Yet the Ecole Hoteliere was so clean that it almost could compete with a semiconductor fab. The world's best hospitality management school trains future managers for positions in top hotels and restaurants. Its students undergo a rigorous education program. They familiarize themselves with haute cuisine as well as haute finance. But what surprised me most was their daily drive to improve their basic skills: from their personal attire to cutting vegetables julienne style. Their motto is simple: you can only become a real leader if you excel in the basics.

That simple adage is certainly valid for microelectronics; yet it is too often forgotten. Many young engineers stare at the pundits receiving prizes and titles, and they question how to reach that level. Do top engineers have some special DNA to analyze complex problems? While the youngsters are pondering how to improve their skills, the answer is often in their first-year lectures. The main difference in quality between average and excellent engineers is a deeper level of understanding the basic principles.

For every engineering activity, other principles are relevant. A printed circuit board designer should be familiar with the interaction among the board material, the wiring, the components, and the mounting technology. His excellence depends on his experience with various technologies and correctly interpreting information such as that found in data sheets. That includes knowledge of the component's behavior within the specification range but more so what happens if the part is pushed outside its operating region during switching sequences, power issues, and other unforeseen events.

Their motto is simple: you can only become a real leader if you excel in the basics.

In any sort of chip design, the principles of mathematics and physics are indispensable. Mathematical transformations allow different views on the sequence of events. The Fourier frequency transform is the basis of signal filtering, sampling theory, image compression, and many more. Time sequences are interpreted as counts per unit time. To transform from time to frequency, the assumption is used that the signal window can be repeated indefinitely.

That's trivial. Now suppose there is only 1 µs of signal available and no option to stretch into infinity. How accurate can the frequency content then be determined? This simple engineering question reveals a basic transformation constraint: a limited observation period results in limited frequency accuracy. Heisenberg's uncertainty theorem is the quantum mechanical consequence. Many physical and engineering effects are directly related to underlying mathematical theories.

Another vital principle involves a first-order system characterized by a time constant. Any source that fills a container by means of a flow that is proportional to the level difference results in an exponentially declining behavior of the flow. That is true for RC and RL circuits, for heating objects, in financial planning, and in metrological phenomena. Even your toilet tank behaves at some moment as a first-order network.

A time constant is a time delay below the cut-off frequency. The delay equals the time constant, and above the cut-off frequency, the delay is a quarter of the signal frequency period. So a 1-µs time constant delays a 2-mHz or a 10-kHz signal by 1 µs. A complex circuit often reveals its behavior by simply checking the time constants of the nodes that the signal will pass. Automated financial speculation techniques feed the flow of commodity prices (copper, corn, oil) into two separate first-order systems. The decision to buy/sell depends on the sign of the difference between the two first-order systems. The financial know-how is in the choice of the time constants for first-order systems.

Mastering this seemingly simple undergrad material to a deeper level is key for reaching some level of excellence. Electrical engineers should improve their basic skills just as junior hotel managers do: pay attention to them every day!

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Ali Sheikholeslami

Capacitor as a Resistor

Welcome to the 14th article in the "Circuit Intuitions" column series. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. I would appreciate your comments and feedback as well as your requests and suggestions for future articles in this series. Please e-mail your comments to ali@ece.utoronto.ca.

About 140 years ago, James Clerk Maxwell, who is well known today for his Maxwell equations, wrote *A Treatise on Electricity and Magnetism* (see Figure 1). In this book, he explained how a capacitor and a switch act effectively as a resistor. It was not known at the time that, 100 years later, this idea would form the essence of a class of ICs known as switched-capacitor circuits. This article reviews Maxwell's basic idea of how to implement a resistor using a capacitor and a switch and how to employ them in the design of a simple integrator.

Figure 2(a) shows a resistor R that is connected to voltage sources V_1 and V_2 on its two terminals. Given Ohm's law, there will be a continuous-time current I that flows through the resistor

$$I = \frac{V_1 - V_2}{R}. \tag{1}$$

Figure 2(b) shows a capacitor C with one terminal grounded and the other one connected either to a voltage source V_1 on the left or to a voltage

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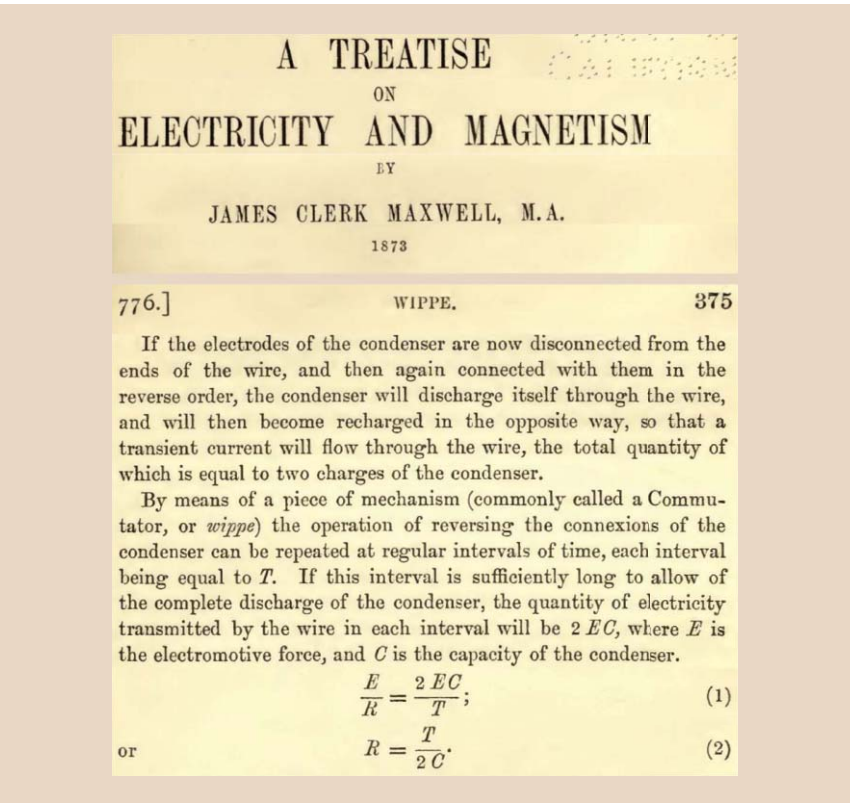

A TREATISE
ON
ELECTRICITY AND MAGNETISM
BY
JAMES CLERK MAXWELL, M.A.
1873

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If the electrodes of the condenser are now disconnected from the ends of the wire, and then again connected with them in the reverse order, the condenser will discharge itself through the wire, and will then become recharged in the opposite way, so that a transient current will flow through the wire, the total quantity of which is equal to two charges of the condenser.

By means of a piece of mechanism (commonly called a Commutator, or *wippe*) the operation of reversing the connexions of the condenser can be repeated at regular intervals of time, each interval being equal to T. If this interval is sufficiently long to allow of the complete discharge of the condenser, the quantity of electricity transmitted by the wire in each interval will be $2EC$, where E is the electromotive force, and C is the capacity of the condenser.

$$\frac{E}{R} = \frac{2EC}{T}; \tag{1}$$

or

$$R = \frac{T}{2C}. \tag{2}$$

FIGURE 1: The front cover and excerpts from Maxwell's book, published in 1873.

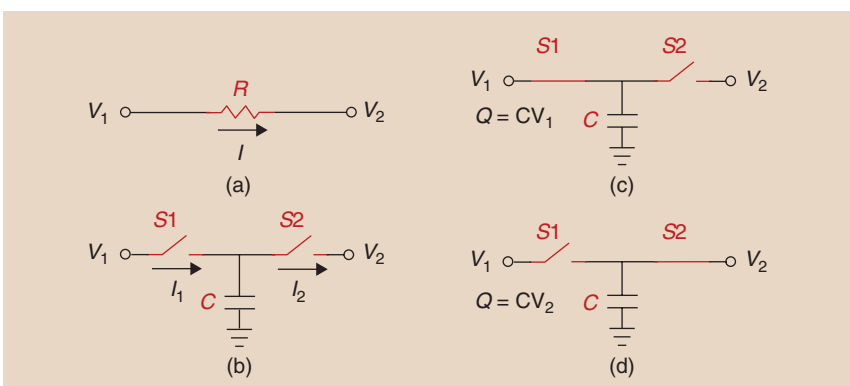

FIGURE 2: (a) A simple resistor, (b) a capacitor and two switches that act like a resistor, (c) the switched-capacitor circuit when S1 is closed and S2 is open, and (d) the switched-capacitor circuit when S1 is open and S2 is closed.

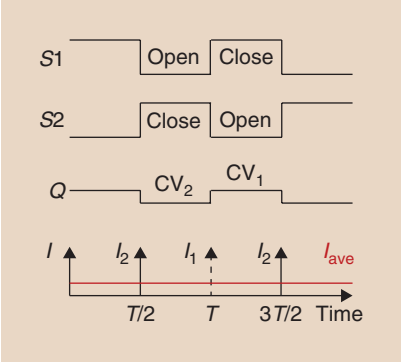

FIGURE 3: The states of S1 and S2, the amount of charge on the capacitor, and the current from V_1 to capacitor (I_1) and from capacitor to V_2 (I_2) as functions of time.

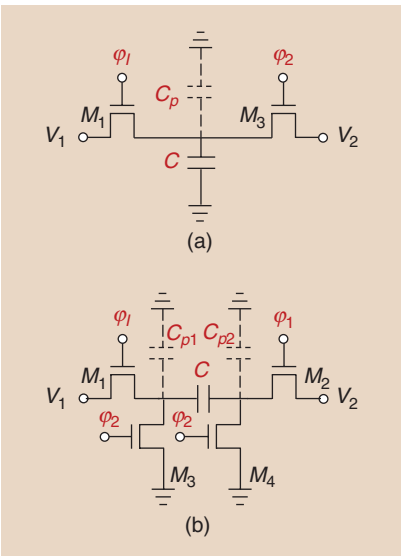

FIGURE 4: (a) A straightforward implementation of a switched-capacitor circuit implementing a resistor using NMOS transistors and (b) a parasitic-insensitive switched-capacitor circuit implementing a resistor.

source V_2 on the right via two switches S1 and S2, respectively. The assumption is that these two switches are turned on and off in a periodic but nonoverlapping fashion. This is illustrated in Figure 3, where S1 is on and S2 is off, and vice versa. Also, note that we have denoted by T the period of switching.

As an example, consider the case where $V_1 > V_2$. In the first half of the period, the capacitor is connected to V_1 [see Figure 2(c)], acquiring a charge of $Q_1 = CV_1$. In the second half, it transfers part of this charge ($C(V_1 - V_2)$) to V_2 [see Figure 2(d)] so as to store a total charge of $Q_2 = CV_2$. In the next cycle, as the capacitor is connected to V_1 again, the capacitor will replenish its charge back to CV_1 level, drawing a charge of $C(V_1 - V_2)$ from voltage source V_1, and transfers this charge to V_2. In steady state, in each cycle, we transfer a charge of $C(V_1 - V_2)$ from V_1 to V_2. Accordingly, the average rate of charge transfer (or average current) from V_1 to V_2 can be found as

$$I_{\text{ave}} = \frac{C(V_1 - V_2)}{T}, \tag{2}$$

which can be rewritten as

$$I_{\text{ave}} = \frac{V_1 - V_2}{T/C}. \tag{3}$$

One immediately notices the similarity of this equation with (1) and may conclude that the switched-capacitor circuit as shown in Figure 2(b) is effectively acting like a resistor with the following equivalent resistance:

$$R_{\text{eq}} = \frac{T}{C}. \tag{4}$$

The fact the equivalent resistance is proportional to T but inversely proportional to C makes intuitive sense. If we increase C, the average current would be larger, corresponding to lower equivalent resistance. However, if we increase T, we are transferring the same charge over a longer period, reducing the current, corresponding to increasing the resistance.

There are a few caveats, however, that one must consider in using a switched capacitor as a resistor.

- We assumed the input V_1 and V_2 are dc voltages. The circuit behaves similarly if V_1 and V_2 are time varying as well, as long as they change much slower than the rate of switching.
- A switched-capacitor circuit is equivalent to a resistor only in the sense that their average currents are the same, but not their instantaneous current. For example, for a fixed V_1 and V_2, the average current leaving voltage source V_1 is dc whereas the corresponding instantaneous current in a switched capacitor is a sequence of delta functions as shown in Figure 3.

At the time when Maxwell published his famous book, he envisioned that one should use "commutators," or "wippe" as they were called at his time, to implement the switches. But for the past few decades, we have been using transistors to implement the switches. We show one implementation of a simple switched capacitor in Figure 4(a) where each switch is replaced by an NMOS transistor. To turn the switch on or off, we rely on the nonoverlapping clock phases that drive the gates of the transistors. At first glance, this seems like an accurate implementation of the ideal switched capacitor circuit shown in Figure 2(b). However, if we take into account the transistor parasitic capacitances, modeled as C_p in Figure 4(a), the effective capacitance becomes $C + C_p$, making the equivalent resistance, as calculated by (4), sensitive to the parasitic capacitances.

Also, as the switches are no longer ideal, they have their own resistances when they are on. These resistances will prevent the capacitors from being charged or discharged instantly, and therefore, one must ensure that $T/2$ is long enough for the capacitor to fully charge or discharge to their intended levels.

To remedy the sensitivity to parasitics, the modern designs use the circuit shown in Figure 4(b). Note that we now use four transistors instead of two. During one phase of the clock (ϕ_1), we turn on M1 and M2, and during the next phase we turn on M3 and M4. Readers are encouraged to figure out why the equivalent resistance of this circuit is also governed by (4) and why this implementation is less sensitive to transistor parasitics. To read more about this, see [1].

Let us now employ our newly built resistor in the design of an integrator. Figure 5(a) shows the integrator design that most of our readers are familiar with. The design uses an op-amp with a capacitor in the feedback loop. Assuming a virtual ground at the common node of the capacitor and the resistor, the current through the resistor, $v_{\text{in}}(t)/R$, will be integrated by the capacitor to

(continued on p. 59)

Behzad Razavi

The Flash ADC

Flash analog-to-digital converters (ADCs) find wide application both as stand-alone components and as building blocks of more complex systems. This architecture dates back to at least the early 1960s. For example, in a patent filed in 1963, Stephenson [1] describes the "parallel" ADC as a known technique. In this article, we study the properties and design issues of this topology.

Basic Architecture

To convert an analog signal to digital form, we can compare its value against a number of equally spaced reference voltages that span the expected range of input amplitudes. Shown in Figure 1, an N-bit flash ADC employs 2^N comparators along with a resistor ladder consisting of 2^N equal segments. The sampling function, which is necessary for conversion from continuous time to discrete time, can be realized within the comparators or as an explicit operation preceding this circuit. In response to $V_j < V_{in} < V_{j+1}$, comparators number one through j produce a logical one at their outputs and the remaining, a logical zero. This "thermometer code" is then converted to a binary or gray output.

The simplicity and elegance of this architecture make it suitable for various conversion rates so long as the speed–power tradeoff remains linear. A favorable tradeoff is obtained if the ADC incorporates a comparator topology with zero static power—a StrongArm latch [2]–[4], for example. As explained below, the ladder's static current is ultimately chosen according to the conversion speed.

Design Issues

The principal drawback of the flash ADC is the exponential growth of its "cost" as a function of resolution. The cost includes power consumption, input capacitance, comparator kickback noise, chip area, and difficulties in routing the signals. We elaborate on some of these issues here.

Suppose we wish to double the resolution of a 5-b flash stage. The analog least-significant bit (LSB) value is halved and so must be the comparator voltage. Using the MOS threshold mismatch equation $\Delta V_{TH} = A_{VTH}/\sqrt{WL}$, where A_{VTH} is a constant and WL denotes the channel area, we observe that WL must quadruple. Since the number of comparators is also doubled, the input capacitance rises by a factor of eight. This trend underscores the need for comparator offset cancellation for resolutions of 4 b and above.

The kickback noise of the comparators also becomes problematic as the resolution increases. This noise arises on each clock edge, as the comparators' input transistors couple internal transitions to the input terminals. Consider, as an example, the StrongArm latch input path shown in Figure 2. We identify two kickback mechanisms: 1) when nodes X and Y fall, they draw a transient current from the inputs through C_{GD1} and

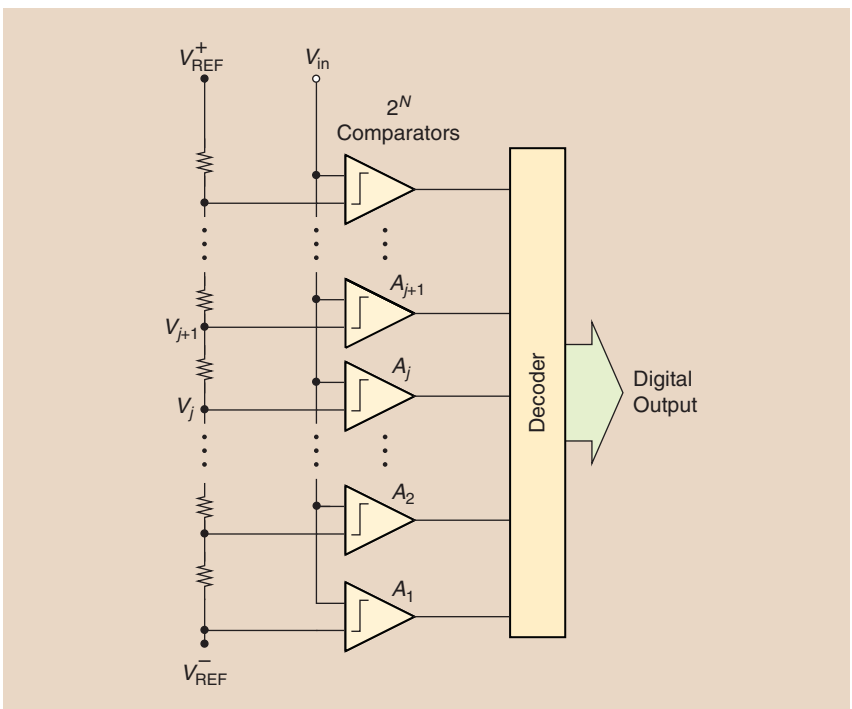

FIGURE 1: The flash architecture.

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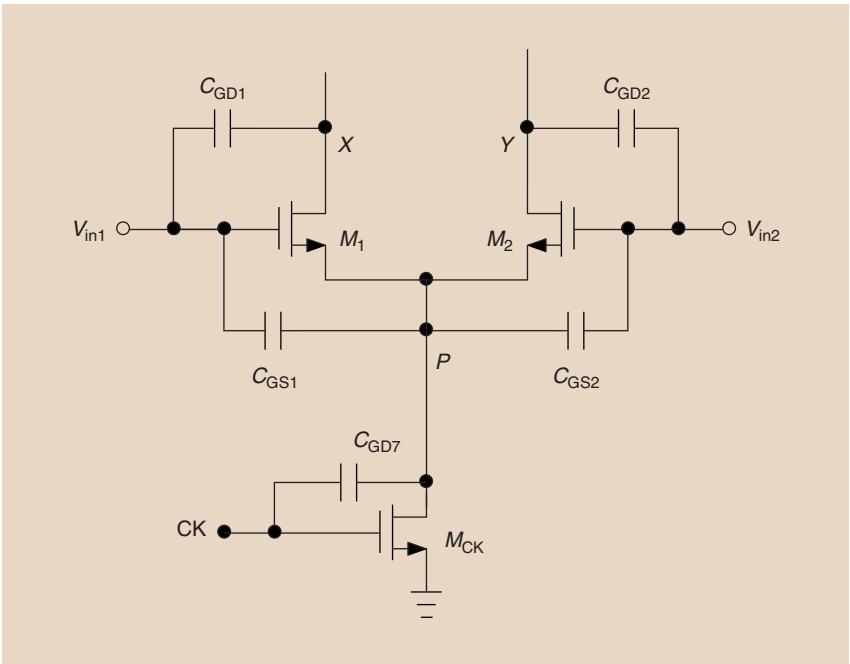

FIGURE 2: The input stage of a StrongArm latch.

C_{GD2}, a significant effect as M_1 and M_2 enter the triode region and these capacitances increase, and 2) when CK goes high, M_{CK} turns on, drawing a transient current from C_{GS1} and C_{GS2} before V_P falls enough to turn M_1 and M_2 on. Note that both effects intensify as M_1 and M_2 are chosen wider so as to reduce the comparator offset. The trouble with kickback noise is that it corrupts the conversion of the present sample and/or lasts long enough to affect the next sample.

The kickback noise currents drawn from V_{in1} and V_{in2} in Figure 2 contain a significant differential component, leading to a differential error voltage if this component flows through a finite impedance. This is inevitable as the kickback sees either the ladder or the ADC input buffer. Consider the single-ended model shown in Figure 3, where $I_1, \ldots, I_n$ model the comparators' kickback noise and are assumed approximately equal. Using superposition, it can be shown that the voltage disturbance at node j on the ladder is given by

$$V_j = \frac{(n-j)j}{2} I_u R_u, \tag{1}$$

where I_u is the value of $I_1, \ldots, I_n$, and R_u the ladder unit resistance. The greatest error occurs at $j = n/2$ and is equal to $(n^2/8) I_u R_u$. To maintain this disturbance below 1 LSB, R_u must be sufficiently small, dictating a lower bound for the ladder's power consumption. It is interesting to note that this power is, in fact, proportional to the sampling rate because, at higher speeds, the kickback noise has less time to subside, and vice versa.

One can precede a comparator design such as the StrongArm latch with a continuous-time differential pair to reduce both the input-referred offset and the kickback noise, but at the cost of considerable power penalty. The kickback noise currents in Figure 3 ultimately flow from V_{REF}^- and V_{REF}^+, demanding that these voltages have a low impedance. This issue translates to a high power dissipation in the reference buffers. One can place a capacitor between these two nodes, but the value of such a capacitor must be very large; otherwise, it slows down the settling of the ladder voltages.

Another difficulty in flash ADC design relates to the appearance of "bubbles" in the thermometer code. Suppose the offset of comparator number j, V_{osj}, in Figure 1 exceeds 1 LSB. Then, for

$$V_{j+1} < V_{in} < V_j + V_{osj}, \tag{2}$$

this comparator and comparator number $j+1$ produce a zero and a one, respectively, leading to a thermometer code of the form ...11010.... Called a bubble, the out-of-place zero generated by comparator number j can create large errors as it travels through the decoder. We generally employ some means of bubble correction; for example, we can detect this situation and swap the outputs of comparators j and $j+1$ [5]. Alternatively, the decoder can simply count the total number of ones in the thermometer code and deliver the result as the final output.

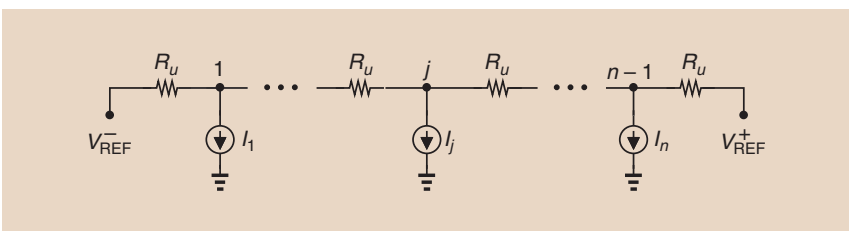

FIGURE 3: A model of kickback noise injected into the ladder.

Fully Differential Design

In most applications, the ADC must digitize a differential analog input, necessitating that the comparators compare this signal to a differential reference. Figure 4(a) illustrates one approach, where a StrongArm latch incorporates two differential pairs that produce currents proportional to $V_{in1} - V_{r1}$ and $V_{in2} - V_{r2}$, with V_{r1} and V_{r2} representing differential reference voltages. These currents are summed at the drains of $M_1 - M_4$ to yield $I_1 - I_2 \propto (V_{in1} + V_{r2}) - (V_{in2} + V_{r1}) = (V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$.

The topology of Figure 4(a) entails three issues. First, the common-mode (CM) level of V_{r1} and V_{r2} must

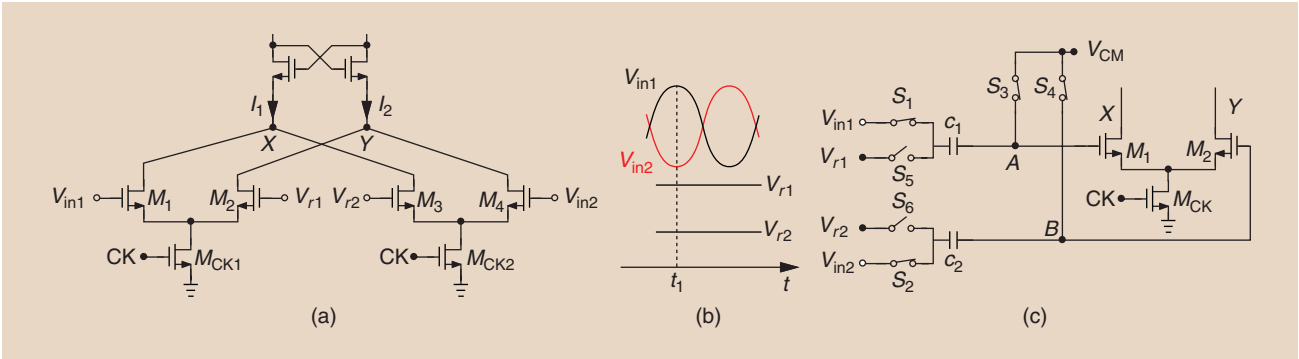

FIGURE 4: (a) A comparator input stage based on two differential pairs, (b) the effect of different CM levels, and (b) an alternative input stage.

accurately track that of V_{in1} and V_{in2}. To see this point, we note in Figure 4(b) that, even if $V_{in1} - V_{in2} \approx V_{r1} - V_{r2}$ at $t = t_1$, each differential pair experiences a heavy imbalance and suffers from a low transconductance. As a result, the mismatches at nodes X and Y and beyond contribute a higher input-referred offset. Second, the circuit introduces four devices, M_1–M_4 at the input and must therefore deal with the offsets of two differential pairs. Specifically, we have $I_1 - I_2 \propto (V_{in1} - V_{in2}) - [(V_{r1} - V_{os1}) - (V_{r2} - V_{os2})]$, where V_{os1} and V_{os2} denote the offset voltages of $M_{1,2}$ and $M_{3,4}$, respectively. Third, the input CM range of the circuit has a lower bound given by V_{GS1-4} and the voltage headroom necessary for M_{CK1} and M_{CK2}. This issue limits the flash ADC's full-scale range, especially at low supply voltages.

Shown in Figure 4(c) is an alternative fully differential input stage that ameliorates the foregoing difficulties. Here, a single differential pair senses an input difference produced by the input switching network and given by $(V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$. In other words, this circuit performs the subtraction in the voltage domain [while in Figure 4(a), it is done in the current domain]. The comparator operates in three phases. First, CK is low, S_1–S_4 are on, and the input network samples the analog signal on C_1 and C_2. Next, these switches turn off and S_5 and S_6 turn on, producing at A and B a voltage difference nearly equal to $(V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$. With a slight delay, CK then goes high to activate the comparator core circuit. This delay is necessary to guarantee that $V_A - V_B$ departs significantly from zero before M_1 and M_2 begin to amplify.

In contrast to the structure of Figure 4(a), the input stage shown in Figure 4(c) deals with the offset of only one differential pair and does not require accurate tracking between the input and reference CM levels. Furthermore, capacitive coupling in this arrangement allows rail-to-railinputswings. Yet another advantage is that the analog sampling provided by C_1 and C_2 in Figure 4(c) obviates the need for a lumped front-end sampler for the ADC. On the other hand, the clocking and X and Y discharge actions in Figure 4(a) tend to *integrate* the input and hence "smear" the sampling point, generally necessitating that the ADC employ an explicit sample-and-hold circuit.

The principal drawback of the flash ADC is the exponential growth of its "cost" as a function of resolution.

The use of the sampling network in Figure 4(c) does raise the input capacitance presented to the analog input. To ensure negligible attenuation of $(V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$, C_1 and C_2 must be chosen much greater than the capacitances seen at A and B. For example, suppose $C_1 = C_2 = 5C_{in}$, where C_{in} includes the gate capacitance of the differential pair and the drain capacitance of S_3 (or S_4). This means that the input capacitance in the sampling mode is more than five times that in Figure 4(a). When S_5 and S_6 turn on, V_{AB} reaches $[(V_{in1}-V_{in2}) - (V_{r1}-V_{r2})][C_1/(C_1+C_{in})] = (5/6)[(V_{in1}-V_{in2})-(V_{r1}-V_{r2})]$, exhibiting a loss of about 17%.

It is possible to reduce the capacitance presented to the analog input by changing the switching sequence in Figure 4(c). We first turn on S_3–S_6 to sample the differential reference on the capacitors and then turn off these switches and turn on S_1 and S_2. The differential voltage thus generated between A and B is the same as before, but the capacitance seen by V_{in1} and V_{in2} is now given by the series combination of the input capacitors and C_{in}. This approach, however, faces two drawbacks: 1) C_1 and C_2 load the resistor ladder, causing a long settling time for V_{r1} and V_{r2}, and 2) the circuit no longer samples the analog input, requiring a front-end sampler for the ADC. A similar timing is described in [6].

Flash ADC Variants

A number of architecture and circuit techniques have been invented to ease the tradeoffs in flash stages. We study two here.

Recall that the input capacitance of the converter grows rapidly with

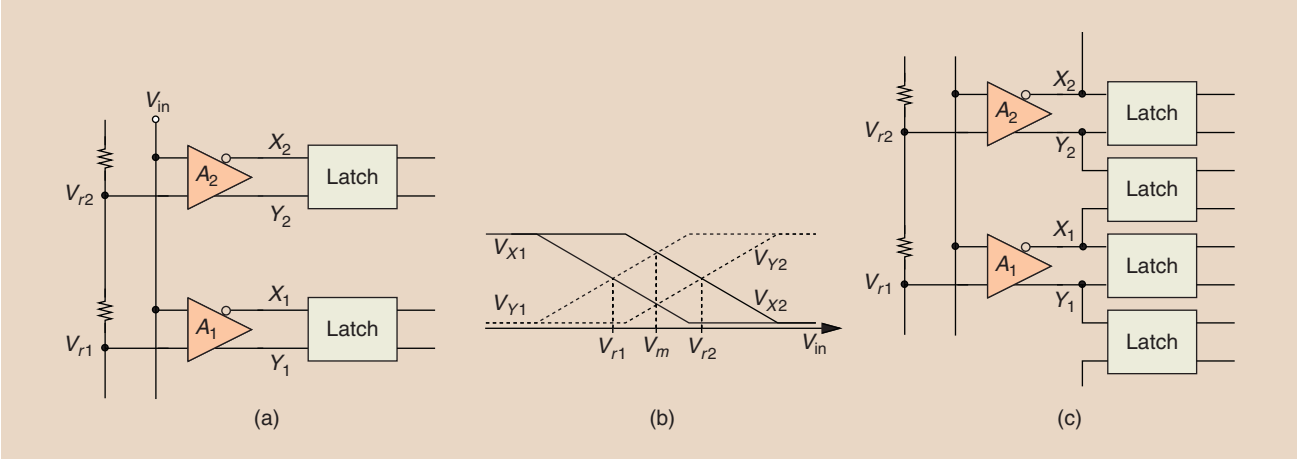

FIGURE 5: (a) A flash stage showing comparators' input differential pairs, (b) characteristics provided by the differential pairs, and (c) a flash stage using interpolation.

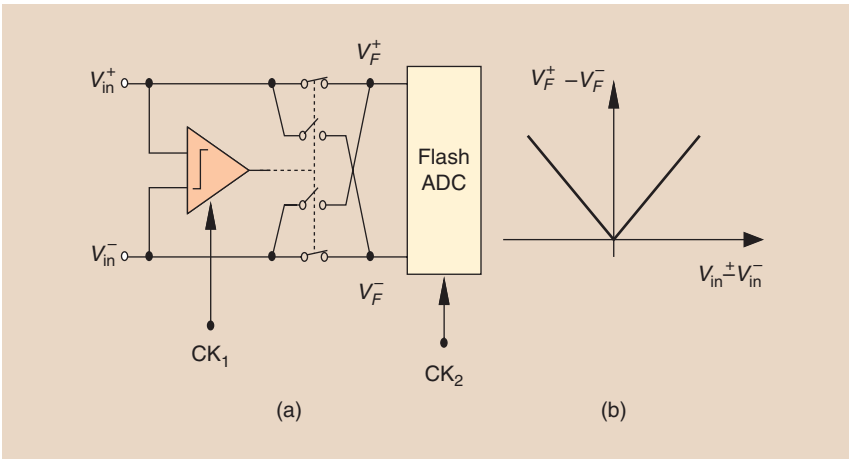

FIGURE 6: (a) A flash stage preceded by a polarity detector and (b) the resulting characteristic.

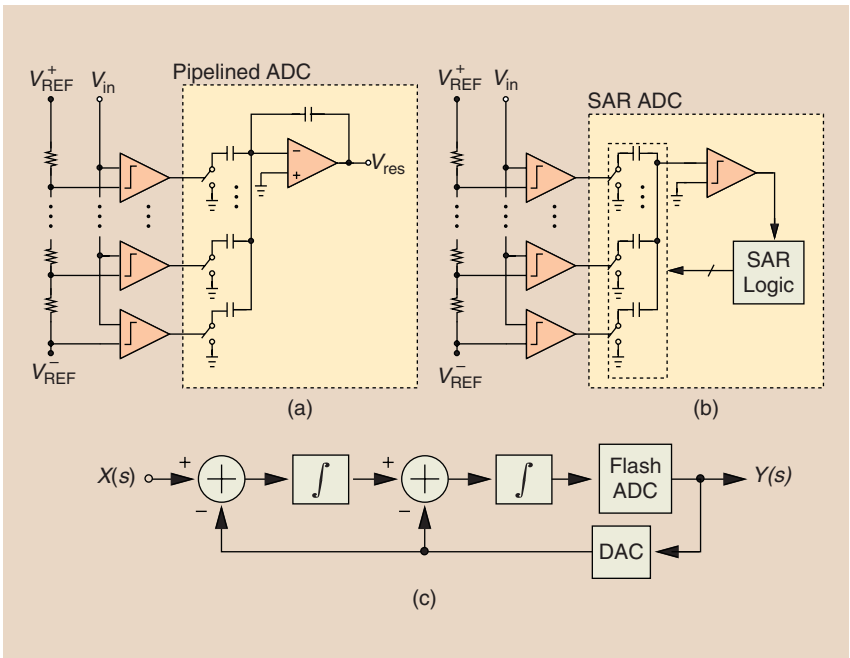

FIGURE 7: The use of flash stages in (a) pipelined converters, (b) SAR ADCs, and (c) $\Delta\Sigma$ modulators.

the resolution. It is possible to alleviate this issue through the use of interpolation. In this context, we view each comparator as a differential pair followed by a latch. Let us first examine the differential pair outputs in Figure 5(a) as V_{in} varies from below V_{r1} to above V_{r2}. Noting that $V_{X1} = V_{Y1}$ for $V_{in} = V_{r1}$ and $V_{X2} = V_{Y2}$ for $V_{in} = V_{r2}$, we can construct the characteristics shown in Figure 5(b). Now, we recognize that $V_{X1} = V_{Y2}$ at $V_{in} = V_m = (V_{r1} + V_{r2})/2$. That is, a latch sensing these two voltages (or V_{Y1} and V_{X2}) can detect when V_{in} crosses midway between V_{r1} and V_{r2}. As depicted in Figure 5(c), the "interpolating" flash [7] architecture doubles the resolution without doubling the number of differential pairs.

The performance improvement afforded by interpolation appears almost free, but it does require that the comparators include a differential pair and suffer from its power dissipation. In particular, a simple StrongArm latch would not suffice for the comparator design in this environment.

Another approach to reducing the complexity and power is illustrated in Figure 6(a) [8]. Here, a front-end comparator detects, under the command of CK_1, the *polarity* of $V_{in}^+ - V_{in}^-$ and accordingly routes the inputs through two of the switches such that the flash stage always senses a positive differential value. Plotted in Figure 6(b), the resulting characteristic

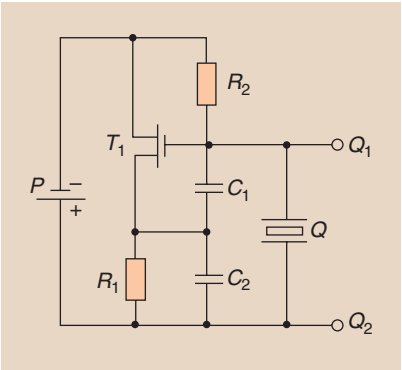

FIGURE 8: The MOS crystal oscillators patented by Luscher.

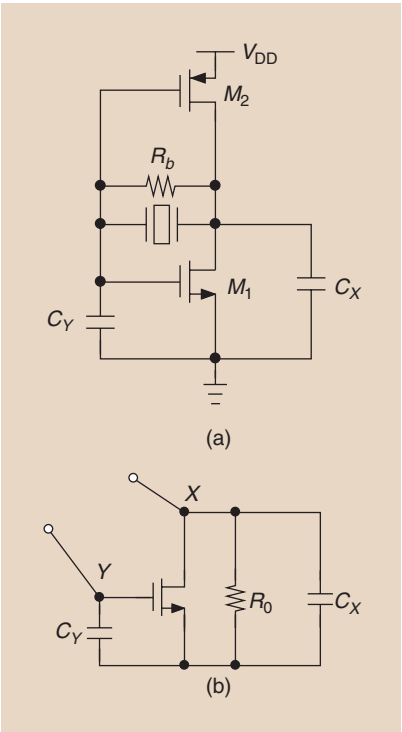

FIGURE 9: (a) A three-point oscillator using an inverter and (b) its simplified model.

is an example of "folding" and produces the most significant bit. Once $V_F^+ - V_F^-$ settles, CK_2 strobes the flash ADC so as to generate the remaining bits. We observe that the overall input capacitance, power, and complexity are approximately halved as the number of comparators drops from 2^N to $2^{N/2} + 1$. These benefits accrue at the cost of more than twofold reduction in speed: not only must the front-end comparator respond to an input difference of, say, 0.5 LSB and activate the proper switches, but also $V_F^+ - V_F^-$ must also settle while the switches drive the input capacitance of the flash stage. Note that the offset of the front-end comparator must remain lower than 1 LSB.

Applications

Flash ADCs exhibit a favorable tradeoff between speed and power dissipation at low resolutions, e.g., in the range of 4–6 b. As such, they prove useful in extremely high-speed applications, e.g., in optical communication receivers that deal with high-order modulation schemes such as 64 quadrature amplitude modulation. Moreover, flash stages can augment other ADC architectures. As shown in Figure 7(a), a flash stage preceding a pipelined converter considerably reduces the magnitude of the residue generated by the first op amp, V_{res}, thereby relaxing its gain, linearity, and output swing requirements. Similarly, as depicted in Figure 7(b), a flash front end can 1) save some clock periods in the convergence of a successive approximation (SAR) ADC and 2) reduce the digital-to-analog converter settling time in the remaining SAR cycles. Another application is in ΔΣ modulators [Figure 7(c)], where a multibit (flash) quantizer lowers both the overall quantization noise and the integrator output swing.

As standalone circuits, flash ADCs perform full conversion in one clock cycle with the aid of massive comparator redundancy, the extreme opposite of how a SAR structure operates. For resolutions up to about 6 or 7 b, the flash topology provides a power-efficient, high-speed solution.

Questions for the Reader

1) In Figure 4(a), why can we not apply V_{in1} and V_{in2} to M_1 and M_2 and V_{r1} and V_{r2} to M_3 and M_4?
2) How does the characteristic shown in Figure 6(b) change if the front-end comparator has an offset equal to 1.5 LSB?

Answers to Last Issue's Questions

1) Estimate the oscillation frequency of Figure 8 if R_1 and R_2 are large.

   The impedance presented to the crystal consists of the series combination of C_1 and C_2 and a negative resistance. This net capacitance must be added to the parallel crystal capacitance in the parallel resonance frequency equation.
2) How does the finite output impedance of M_1 and M_2 in Figure 9 affect the oscillator's performance?

   Since M_1 and M_2 are in parallel, we can return to the three-point oscillator model shown in Figure 9(b) and ask how the finite resistance R_0 affects the startup condition. If R_0 is large, we can transform the parallel combination of R_0 and C_X to a series combination having an equivalent resistance approximately equal to $1/(R_0 C_X^2 \omega^2)$. Thus, this positive resistance weakens the effect of the negative resistance provided by the transistors.

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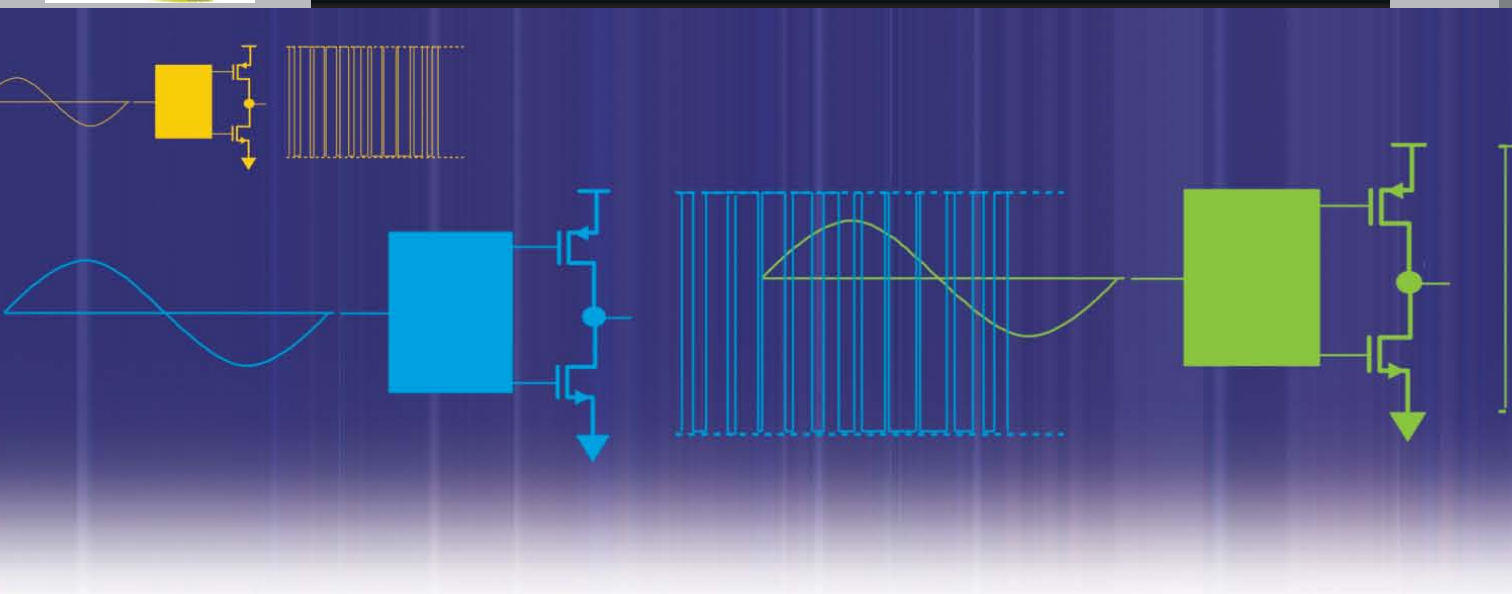

Fundamentals of Audio Class D Amplifier Design

A review of schemes and architectures

Xicheng Jiang

Class D amplifiers [1]–[16], or switching amplifiers, are popular components in mixed-signal IC design and widely adopted for smartphones and tablets with rich multimedia, thanks to the high-efficiency and high-output power capability. Their applications range from audio and video drivers to envelope tracking for power amplifiers.

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Audio Amplifier Classes

Class A amplifiers are the most common type of amplifier class due to their simple design. Class A literally means "the best class" of amplifier because of their low signal distortion levels and are probably the best sounding of all the amplifier classes. Generally, the class A amplifier output stage is never driven fully into its cut-off or saturation regions. Then the transistor never turns "OFF," which is one of its main disadvantages and implies that the efficiency is very low. Efficiency is defined as the average power delivered to the load divided by the power drawn from the supply. The power drawn from the supply includes power delivered to the load and consumed by

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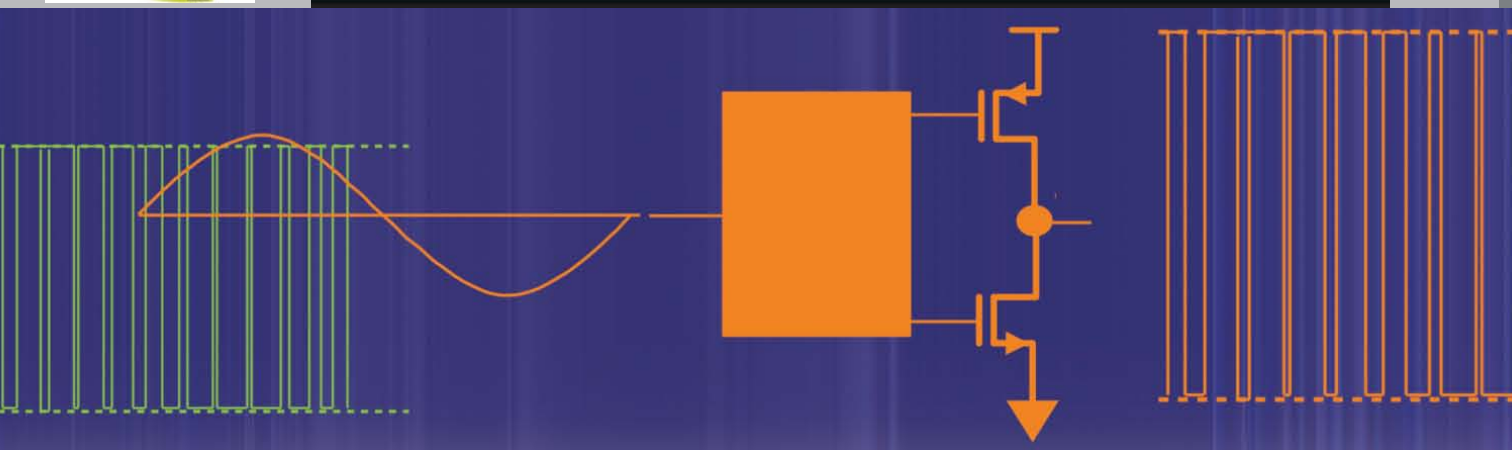

internal circuits. The efficiency can be expressed as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{ckt}}}.$$

A simple class A structure is a source follower as shown in Figure 1. The bottom N-type metal-oxide-semiconductor (NMOS) is biased as a decent current source. The output follows the input except dc level shifting. Class A amplifiers are impractical for professional audio applications due to their low efficiency. Low efficiency implies more power burned on-chip, which can cause heating problems.

Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the class A amplifier. The basic class B amplifier (as shown in Figure 2) uses two complimentary transistors, either bipolar or field-effect transistor (FET) for each half of the waveform with its output stage configured in a "push–pull" type arrangement so that each device amplifies only half of the output waveform. Thus the transistor conducts only half of the time, either on a positive or negative half cycle of the input signal. In the class B amplifier, there is no dc base bias current as its quiescent current is zero, so that the dc power is small and therefore its efficiency is much higher than that of the class A amplifier. However, the price paid for this efficiency improvement is degraded linearity. Neither device is ON in the crossover region, which leads very bad crossover distortion in the output waveform.

We have seen the linearity advantage of class A and the efficiency benefit of class B. We can create a structure called class AB, which offers both high linearity and high efficiency. As its name suggests, the class AB amplifier [1], [2] is a combination of the class A and class B type amplifiers and is currently one of the most commonly used type of audio power amplifier. The class AB amplifier (Figure 3) is a variation of a class B amplifier, except that both devices are allowed to conduct at the same time around the waveform's crossover point, eliminating the crossover distortion problems of the previous class B amplifier.

The two transistors have a very small bias voltage to bias the transistors just above its cut-off point. Then the conducting device, either bipolar or FET, will be "ON" for more than one-half cycle, but much less than one full cycle of the input signal. Therefore, in a class AB amplifier

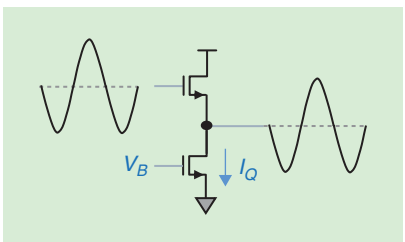

FIGURE 1: A class A amplifier.

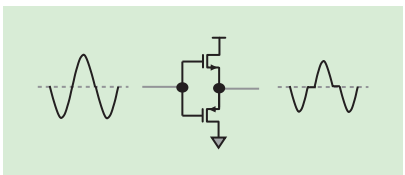

FIGURE 2: A class B amplifier.

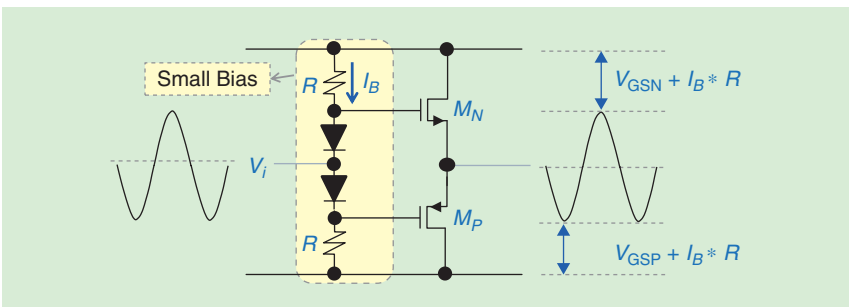

FIGURE 3: A CMOS class AB audio amplifier.

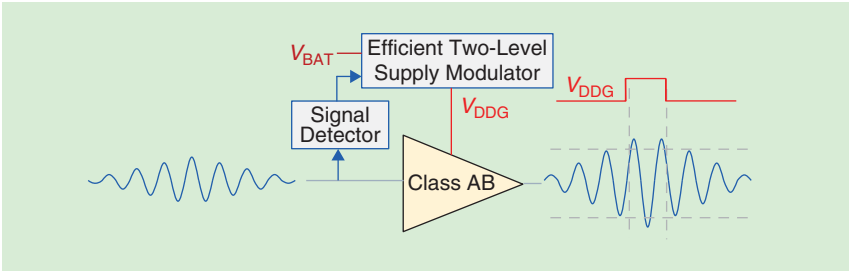

FIGURE 4: A class G amplifier.

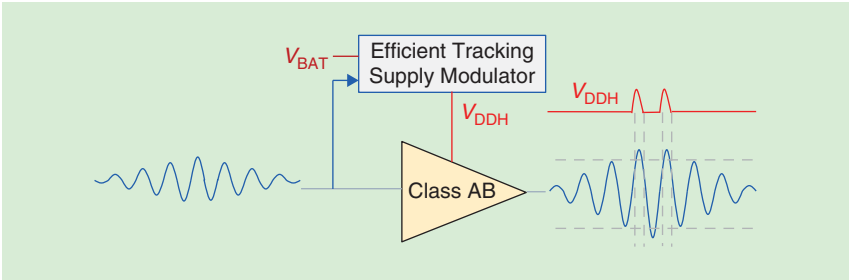

FIGURE 5: A class H amplifier.

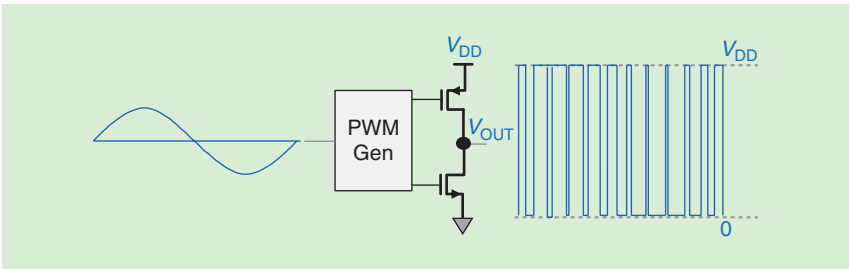

FIGURE 6: A class D amplifier.

design, each of the push–pull transistors is conducting for slightly more than the half cycle of conduction in class B but much less than the full cycle of conduction of class A. The conduction angle of a class AB amplifier is somewhere between 180° and 360°, depending upon the chosen bias point. The advantage of this small bias voltage, provided by series diodes or resistors, is that the crossover distortion created by the class B amplifier characteristics is overcome, without the inefficiencies of the class A amplifier design. So the class AB amplifier is a good compromise between class A and class B in terms of efficiency and linearity.

A drawback of the CMOS class AB output stage is the limited output swing range due to headroom requirements. For certain audio output levels, the higher the audio supply, the lower the efficiency. Typical audio or music has a 10–20–dB crest factor. Crest factor is defined as the ratio of peak amplitude to root-mean-square (rms) level. The minimum CMOS class AB amplifier supply voltage is dictated by the peak audio level, and the audio/music rms level is substantially lower than the peak level. This implies that the class AB amplifier is terribly inefficient in terms of having a fixed supply for audio applications.

The class G topology (Figure 4) uses multiple power supply rails of various voltages and automatically switches between these supply rails as the input signal changes. This constant switching reduces the average power consumption. Class G includes the main class AB amplifier. In addition, it also includes a signal detector and supply modulator. The supply modulator provides discrete supply levels (Vdd, Vdd/2, etc.) depending on signal detector output. Shown in Figure 4 is a two-level class G. It can be three levels or even more. The main difference between class AB and G amplifiers is that conventional class AB amplifiers have a fixed supply and class G amplifiers have a multilevel supply where the supply level is selected based on the signal level. If we continue increasing the number of supply levels to infinite, the class G amplifier becomes a class H. As shown in Figure 5, class H includes the main class AB amplifier. In addition, it also includes a supply modulator that efficiently tracks the audio signal. The efficiency is further improved compared to class G topology, especially when the signal swing is large.

The fundamental limitation for a linear amplifier is that the transistors inside a linear amplifier operate in the saturation or linear region. There is a relatively large voltage drop when a large current passes through the transistor, resulting in a large power loss that inevitably hurts efficiency. Ideally, we want to make output devices into switches where the current and voltage are out of phase. Specifically, when a large current passes an output switch, the voltage drop across the switch is zero (Switch-ON), or when a large voltage drops across a switch, the current pass through the switch is zero (Switch-OFF). This implies there is zero power loss in the output stage. This is basically the principle of class D operation. Class D amplifiers, as shown in Figure 6, first modulate the audio signal in digital or analog format into pulsewidth-modulated signals, and these signals then drive the output switches. The output pulsewidth modulated signals are then filtered by either external filter or by the speak coil itself.

Class D amplifiers theoretically can reach 100% efficiency. Figure 7 shows the efficiency comparison of different classes of amplifiers; the two class G curves represent a two-level class G and a three-level class G. As shown, the three-level class G is more efficient than the two-level class G. As we continue increasing the number of levels to infinite, it becomes class H, i.e.,

the supply level tracks the signal. It is very clear that the class D topology has much better efficiency than linear amplifier classes.

There are several other classes of amplifiers, which are not commonly used but worth mentioning, The class C amplifier has the greatest efficiency but the poorest linearity. The class E/F amplifier uses harmonic resonators in the output network to shape the output waveform into a square wave. Class E/F amplifiers are capable of high efficiencies of more than 90% if infinite harmonic tuning is used. A class I amplifier has two sets of complementary output switching devices arranged in a parallel push–pull configuration with both sets of switching devices sampling the same input waveform. A class S amplifier is a nonlinear switching mode amplifier similar in operation to the class D amplifier. A class T amplifier combines both the low distortion signal levels of a class AB amplifier and the power efficiency of a class D amplifier.

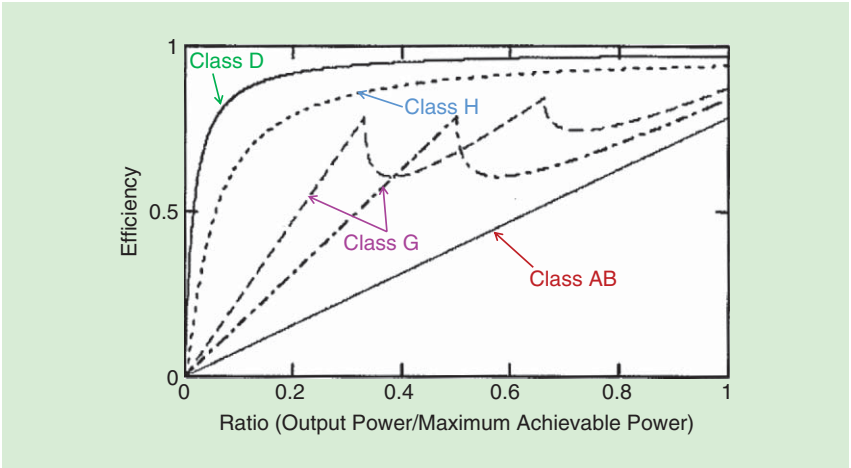

FIGURE 7: An efficiency comparison.

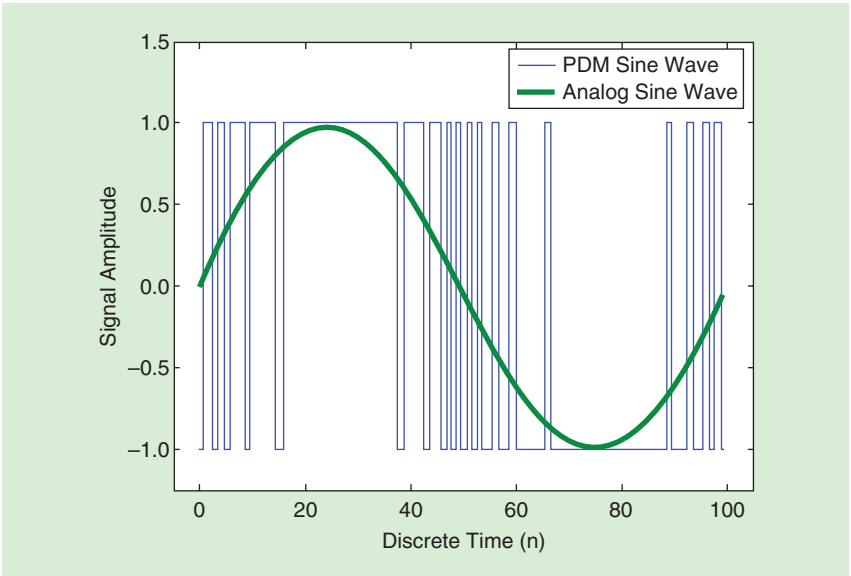

FIGURE 8: A PDM waveform.

Class D Modulation Scheme

The most common class D modulation schemes are pulse-density modulation (PDM) or pulsewidth modulation (PWM). PDM is a form of modulation used to represent an analog signal with a binary signal, and its output is a stream of single bits representing a sample signal. In a PDM signal, specific amplitude values correspond to the relative density. The output of a 1-b digital-to-analog converter (DAC) is the same as the PDM encoding of the signal. Figure 8 shows the PDM waveforms, where the green curve is the input analog sine wave and the blue curve represents the corresponding PDM output waveform. PWM is a special case of PDM where the switching frequency is fixed, as shown in Figure 9. For a 50% voltage with a resolution of 8 b, a PWM waveform will turn on for 128 clock cycles and then off for the remaining 128 cycles. With PDM and the same clock rate, the signal would alternate between ON and OFF every other cycle. The average is 50% for both waveforms, but the PDM signal switches more often. For the 100% or 0% levels, they are the same. Figure 10 shows the typical waveforms of PDM and PWM outputs corresponding around the zero-crossing of the input level. The analog input signal drifts slowly from positive to negative. In this region, the PDM modulator output toggles at an average rate slightly lower than fs/2. For the PWM output, it toggles at the rate of f_{osc}.

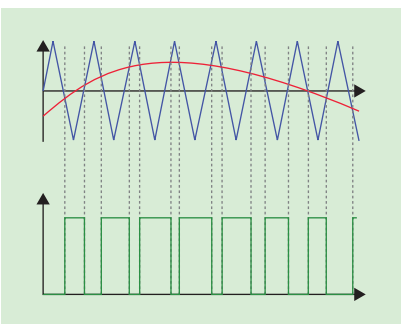

FIGURE 9: A PWM waveform.

The advantage of PWM is that it has a much lower toggling rate, with fewer transitions during any given period of time. This helps reduce the impact of the switching errors and the dynamic power. To realize these benefits, it is desirable for f_{osc} to be as low as possible. Typically PDM has fs in the order of 100 MHz, while the PWM modulator frequency is in the order of a few hundred kilohertz.

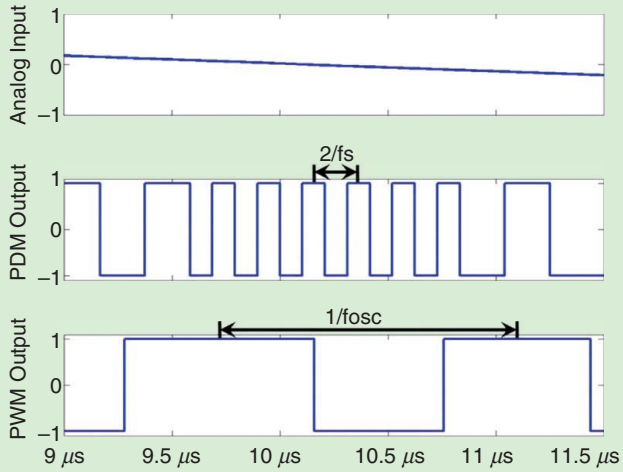

FIGURE 10: A comparison of PDM and PWM waveforms.

For PWM, the two popular modulation schemes are AD and BD modulation. Figure 11(a) shows how the H-bridge operates with an AD modulation scheme, which basically has two states. Figure 11(b) illustrates a class D AD modulation response with zero input. Both OUTP and OUTN toggle at 50% duty cycle, but with different polarities. OUTN is a complementary of OUTP. So when a large voltage level drops across the speaker, even the input is zero. The ramp up and down current waveform corresponds to the quite inductive speaker coil. To preserve the energy, a low-pass for inductor and capacitor (LC) filter is needed. The cut-off frequency should be below the switch frequency. The operation of BD modulation is more interesting. As shown in Figure 12(a), it has four states depending on the input signal conditions: increasingly positive, decreasingly positive, increasingly negative, and decreasingly negative. Figure 12(b) illustrates class D BD modulation response with zero input. Both OUTP and OUTN still toggle at nearly 50% duty cycle, with mostly the same polarities. The differential output has alternative narrow pulses. So only a very small voltage level drops across the speaker when the input is zero. Because of very little current dissipation with zero input, a low-pass LC filter is not required.

When deciding on the architecture of a class D amplifier, it involves the selection of the modulation scheme and the topology. For a modulation scheme, it includes PDM and PWM. PDM has a high pulse rate while PWM has a low pulse rate, good performance, and low power consumption. So PWM is a clear winner. Deciding on digital topology verse analog feedback topology involves the tradeoff between performance and power consumption. Digital implementation has a lower power consumption and also a lower performance, while analog feedback provides good performance at the cost of quiescent power. Depending on the system requirement, it can be a PWM class D amplifier with digital or analog feedback implementation.

Digital PWM Class D

Figure 13 shows the digital PWM architecture [10], [17] consisting of a digital PWM modulator and a switching driver. A digital triangle waveform with an oscillation frequency of 667 kHz is compared to the output of a digital loop filter, the digital comparator is clocked at 24 MHz, and the output of the digital comparator is a PWM signal toggling at the rate of 667 kHz. This PWM signal is fed back within the digital feedback loop of the modulator. Timing distortion errors in the PWM signal, due to the uniform sampling of the comparator, are reduced with the high forward loop gain in this digital feedback loop. The result is that this PWM modulator produces high fidelity PWM signals that are not impacted by the large timing distortion errors from uniform sampling. To fully realize the benefit of PWM, the modulation frequency f_{osc} should be as low as possible with respect to the comparator clock rate. This allows the switching rate to be made as low as possible and reduces the impact of the switching errors

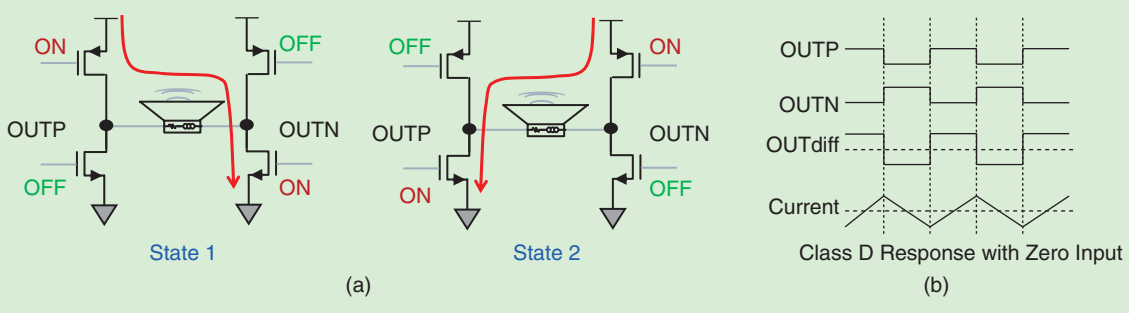

FIGURE 11: (a) An AD modulation scheme and (b) AD modulation waveforms.

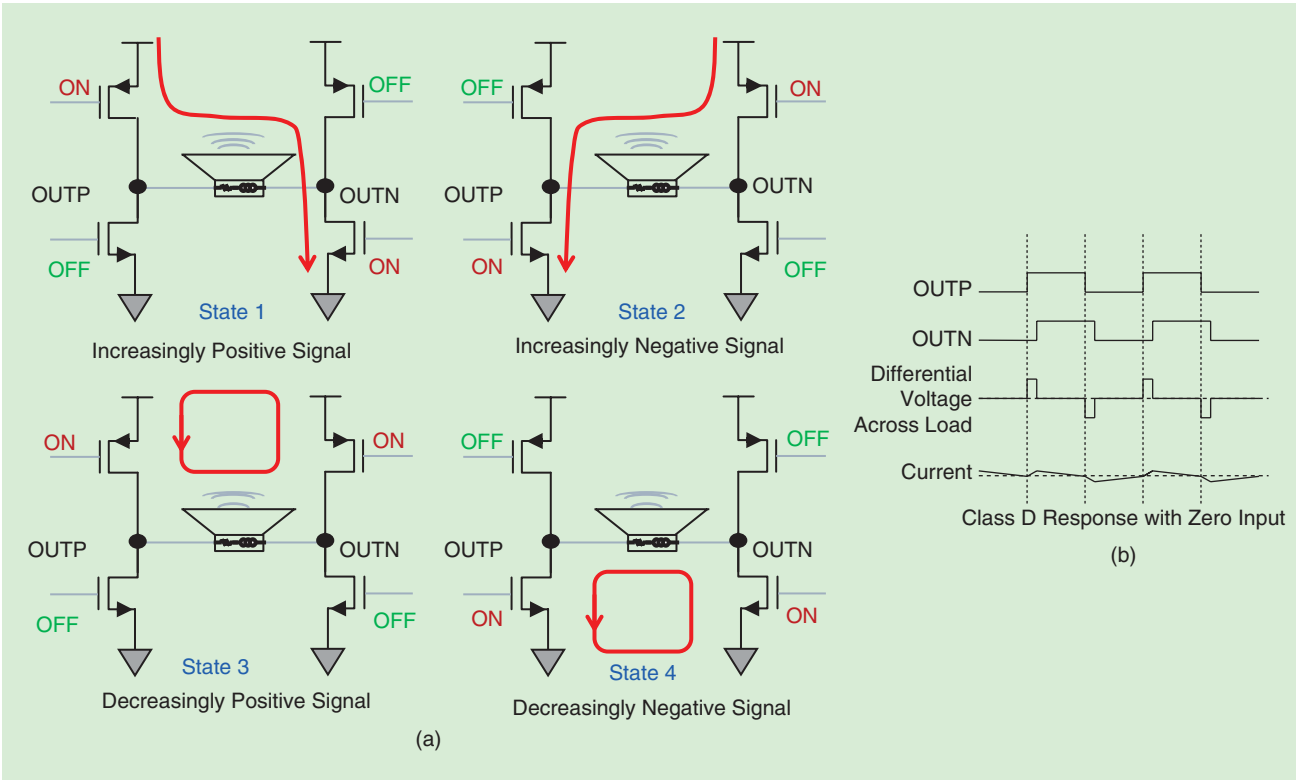

FIGURE 12: (a) A BD/filterless modulation scheme and (b) BD/filterless waveforms.

from the switching driver on performance. The target dynamic range is 120 dB. The digital PWM modulator should be carefully designed, and the analog noise from clock jitter supply should be analyzed and modeled. Of course, digital implementation can offer low quiescent current consumption and there is no need for an analog DAC.

Digital quantization noise is suppressed by the fourth-order digital PWM (Figure 14). The design of the digital PWM follows three major considerations. The first is the spectral shaping of the pulse and timing errors to enhance dynamic range. The second is to maximize the input range for which the modulator is stable. The third is to reduce the switching rate as much as possible. The modulator topology is the cascade-of-integrators with feedback and the two local resonators providing in-band nulls for the optimal noise suppression. The multiple feedback signals from the output are 1 b. The fourth-order noise transfer function has two zeros at 5 and 18 kHz implemented with two local resonators in the modulator loop.

Increasing the modulator order beyond the fourth order does not significantly enhance the quantization noise performance but, rather, decreases the maximum input range for which the modulator is stable. Increasing the ratio of *fs/fosc* improves pulse-width resolution and thus reduces quantization noise. However, the modulator consumes more dynamic power with a higher *fs*. The lower limit of the switching rate *fosc* is restricted by the unity-gain frequency of the loop transfer function. Specifically, the switching rate should not be lower than π times the unity-gain frequency of the loop transfer function. Otherwise, the rate of change of the comparator input signal can exceed the rate of change of the triangle waveform and can saturate the modulator. In this design, the switching rate of the triangle waveform is slightly higher than π times the unity-gain frequency of the loop transfer function. Further reduction of the switching rate either compromises the stability margin or must be accommodated by reducing the bandwidth of the modulator loop, which degrades the spectral shaping.

Nonlinearity of the driver switch, as shown in Figure 15, also impacts the class D driver performance. The finite on-resistance of the driver switch can cause nonlinearity and degrades the power efficiency. The

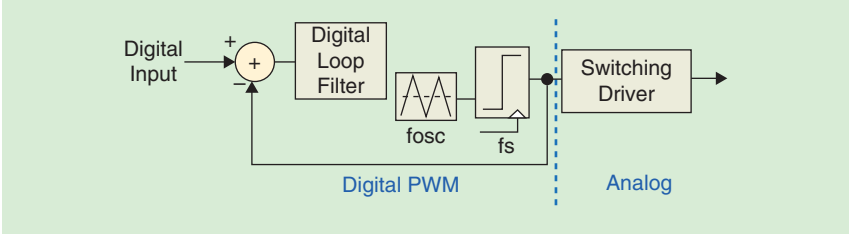

FIGURE 13: A digital PWM class D amplifier.

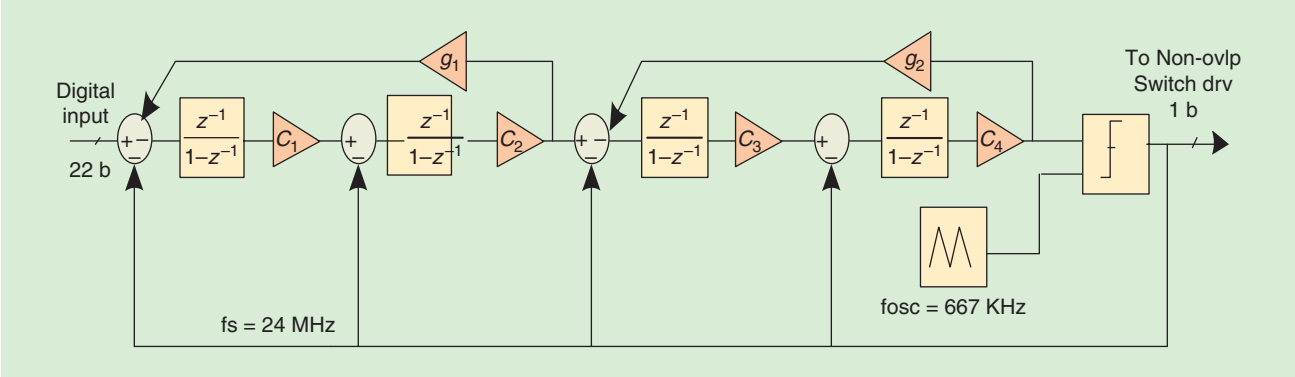

FIGURE 14: A digital PWM modulator.

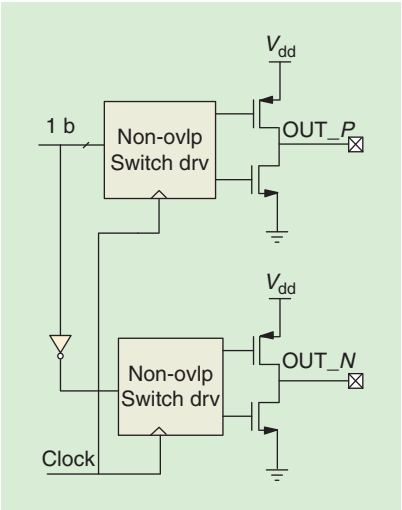

FIGURE 15: A switch driver.

on-resistance of the pMOS and nMOS devices is minimized by using a large width/length ratio. The switch size is optimized to obtain nominal on-resistance of 500 mΩ for each pMOS and nMOS device, which is sufficient to achieve total harmonic distortion (THD) lower than –40 dB at full scale and lower than –80 dB at –10 dBFS. For each half-bridge circuit, the nonoverlap switch driver is designed such that the pMOS and nMOS switches of the same half-bridge will not be turned on at the same time under all conditions. This is essential to avoid crow-bar current. A long overlap time causes distortion.

There is a design tradeoff between the efficiency and the crow-bar current. The nonoverlap times (output) are determined by gate delays in the predriver circuit and are optimized to be long enough to avoid significant crow-bar current. The nonoverlap times are also kept short enough to avoid excessive duration of tristate at the switch driver output, to maintain good distortion performance. The predriver buffers are scaled with a series of gradually increasing buffer sizes to provide optimized fast-switching at the gates of the four large transistors in the output switching driver. The switching time of the output switch should be much shorter than the minimum pulsewidth at the modulator output. The minimum pulsewidth is one clock period of the modulator clock. Excessively slow switching can cause missing pulses, which increases THD. The rising and falling time of the switching driver is lower than 1 ns in this design, which is much shorter than the 41.7-ns modulator clock period.

Analog Feedback Implementation

Shown in Figure 16 is a typical analog feedback class D amplifier [11]–[15] for cellular application. The feedback loop helps to reduce distortion and noise and improve the power supply rejection. High power supply rejection ratio (PSRR) at 217 Hz is critical in a Global System for Mobile communication (GSM) system. The class D amplifier produces pulse-width modulated outputs with fast transition and rail-to-rail swing. Conventional architecture directly feedbacks the class D output to the input of the loop filter, causing large common-mode (CM) variations and a large disturbance at the input of the loop filter. Consequently, the class D amplifier THD+N performance is limited. The loop filter in a conventional class D amplifier processes both signals and errors

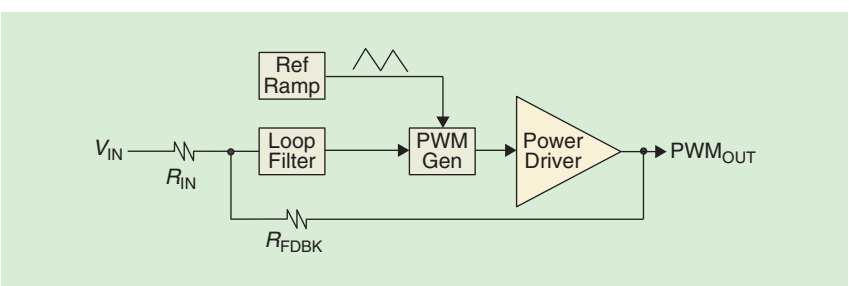

FIGURE 16: Conventional analog feedback class D architecture.

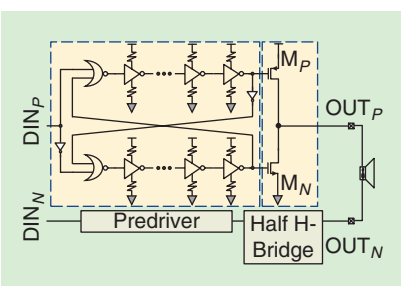

FIGURE 17: Edge rate control for EMI reduction.

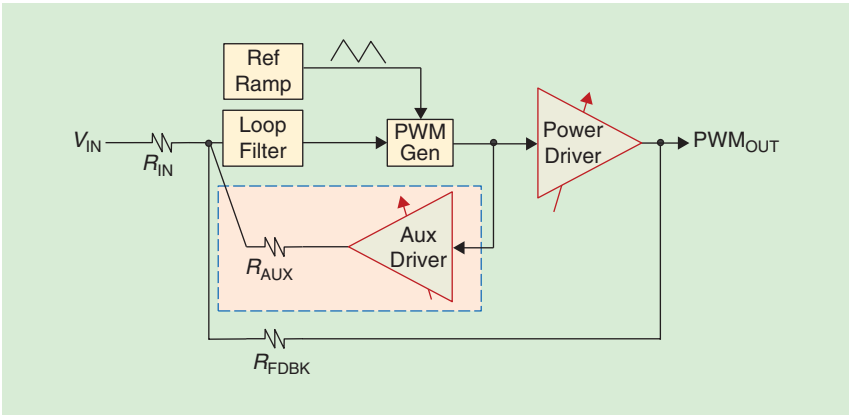

FIGURE 18: A class D amplifier with an auxiliary loop.

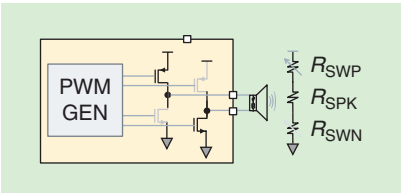

FIGURE 19: Programmable driver strength.

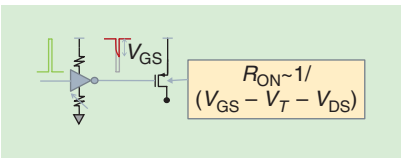

FIGURE 20: Switch-on resistance control.

injected in the loop. The loop filter output includes a large signal swing when the input signal is large. This not only increases the current consumption of the amplifier to support the large output swing but also limits the error correction range before the loop is saturated. For the loop to sufficiently suppress the battery disturbance in the mobile system, the signal level, namely the output power, has to be limited to keep low distortion.

Furthermore, the fast switching time and nearly rail-to-rail signal swing of class D amplifiers result in both high efficiency and troublesome electromagnetic interference, or the so-called EMI. In addition, the large switching current through the speaker coil coupling with the parasitic inductance from the wire-bond package tends to induce large overshoots and undershoots at the amplifier output. To make the device operate reliably, conventional designs reduce the output signal swings by an amount equivalent to the overshoot or undershoot. As a result, existing class D amplifiers with a wire-bond package have very limited output power capability.

An effective EMI reduction approach [6] is shown in Figure 17 with the detailed implementation of the half H-bridge and predriver circuit. The output switching edge rate is controlled by the power switch gate voltage. And the switch gate voltage is provided by the predriver, which consists of a chain degenerated digital gates. Nonoverlapping voltage was provided for P and N switches such that they will not be turned on simultaneously at any given time. The nonoverlapping time was generated to track the slow transition edges. The nonoverlapping time must be larger than the rising/falling time to avoid crowbar current. However, efficiency and linearity may degrade with increased edge rates. Design tradeoffs among efficiency, linearity, and EMI reduction determine the optimal edge rate.

Another unpleasant user experience is the pop/click noise [6] associated with the class D amplifier. The pop/click noise is caused by the unpredictable transient during power up/power down due to abrupt changes of the PWM and the dc offset. To effectively suppress the pop/click noise, an auxiliary loop [6], as shown in Figure 18, is introduced. During power up, the auxiliary loop helps establish the feedback loop. The power driver has the weakest driving strength, which effectively disconnects the speaker from amplifier. So the speaker does not sense any uncomfortable transients. The driving strength of both the auxiliary and power drivers is programmable. Their driving strengths are ramped oppositely during power up and power down. At the beginning of power up, the power driver starts with zero drive strength. At the same time, the auxiliary driver is at full drive strength.

The auxiliary path enables the loop to settle without affecting the output voltage across the speaker. During power up, the strength of the power driver gradually increases until it reaches its maximum, while the strength of the auxiliary driver gradually reduces to zero. This provides a smooth handoff between the auxiliary and main feedback loops. When the loop has settled, the amplifier offset is reflected by the PWM. As a result, both the PWM pulse amplitude and amplifier offset are ramped simultaneously. The power-down procedure is reversed with respect to the ramping process during power up. Figure 19 shows a pair of PMOS and NMOS switches connecting the speaker to the battery and the ground. Even though the speaker is directly connected to the battery, the voltage across the speaker is attenuated by a factor of Rspk/(Rswp+Rspk+Rswn), where Rspk is the speaker resistance and Rswp and Rswn are the on-resistance for the P-switch and the N-switch. A weak driving strength implies large switch on-resistance. To ramp the drive strength, the switch on-resistance can be ramped. Figure 20 conceptually shows a PMOS switch and its gate driving voltage. As the formula indicates, the switching on-resistance is controlled by the gate voltage. The switch gate driver has added source impedance, which slows down the transition. For a narrow pulse input to the predriver, the output pulse amplitude is limited due to the slow transition.

Figure 21 shows the detailed implementation of ramping the driver strength. The right side of the figure

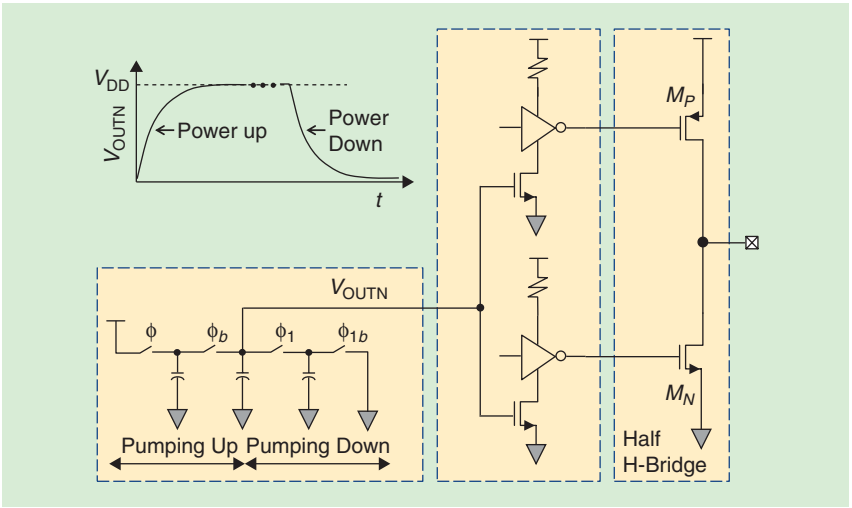

FIGURE 21: Class D power driver ramping.

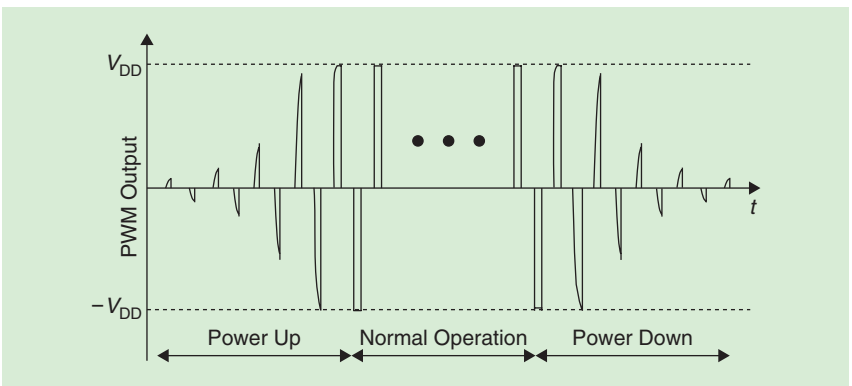

FIGURE 22: The differential PWM pulses during power up and power down.

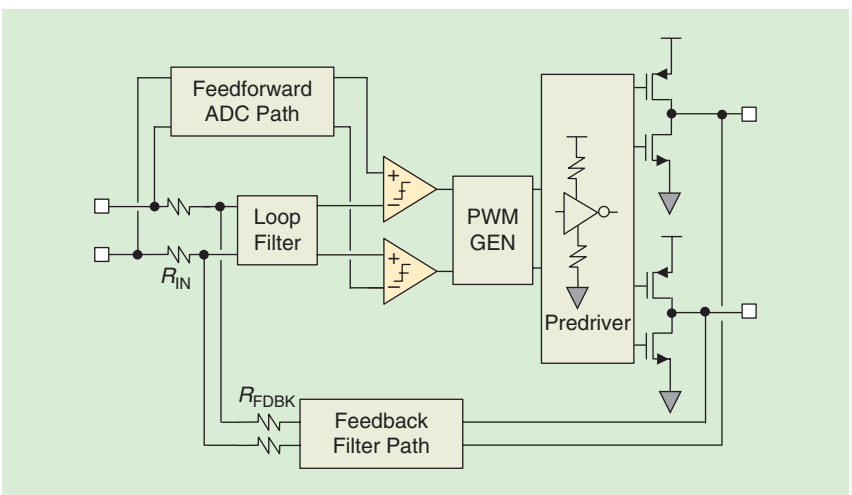

FIGURE 23: The enhanced class D architecture.

is the half H-bridge and its predriver. The source impedance of the predriver is realized with the NMOS transistor operating in the linear region. The gate voltage of the NMOS transistor is slowly ramped with switched capacitor charge pump circuit. During power up, the gate voltage Voutn is slowly ramped up, while during power down, the gate voltage is slowly ramped down. During power up, the gate voltage of the PMOS power switch Mp is slowly ramped down. As a result, the Mp on-resistance is slowly ramped down. The gate voltage of the NMOS power switch Mn is also slowly ramped down, implying that the NMOS switch is firmly turned on initially. As a result, the speaker is firmed tied to ground at the beginning of power up. The differential PWM pulse during power up and power down are shown in Figure 22. Unlike a conventional class D amplifier where the PWM pulses abruptly start with rail-to-rail amplitude, the PWM pulses are slowly ramped up during power up and slowly ramped down during power down. It is worth mentioning that the dc offset is reflected by the width of the PWM pulses. So the effective dc offset is also slowly ramped.

Enhanced analog feedback class D architecture [15], shown in Figure 23, resolves all of the aforementioned issues. It includes a feedforward analog-to-digital converter (ADC) path, feedback filters, and edge rate control in the driver stage. The feedforward path is designed to process the signal, using the loop filter to integrate only the difference between the input and the feedback signals. The loop filter, therefore, mainly responds to errors injected into the loop. This architecture significantly extends the loop filter operation range to support a much larger signal level and, thus, large output power capability. To avoid PSRR performance degradation due to the feedforward architecture, the loop filter, feedback, and feedforward paths are powered from an internal low drop out regulator. The feedforward path basically provides a period modulated ramp signal for PWM generation. This is very different from conventional PWM generation with a period-fixed ramp signal.

The feedforward path, as shown in Figure 24, consists of an ADC, digital PWM, and analog ramp generators. The accuracy requirements for the ADC and analog ramp circuits are relaxed because the feedback loop also attenuates any errors introduced in the feedforward path. The digital

PWM generator converts the ADC outputs to a PWM signal, and the ramp generator transforms the digital PWM signals to analog ramps signals.

Direct feedback of the class D output to the input of the loop filter can induce distortion in the loop filter operation. Since the class D output switches between ground and V_{BAT} while driving a speaker coil, its slew rate is extremely large. Also, it is accompanied by an overshoot and undershoot induced by the speaker coil current and the inductance of the bonding wires of the supply and load rails. Furthermore, the output CM varies widely as the output switches between supply rails. This is unlike a class D amplifier with binary modulation where the output's CM is constant. To reduce the high-frequency intermodulation distortion associated with direct feedback and eliminate the loop filter input CM disturbance from the class D output that has a rail-to-rail CM variation, the feedback path (Figure 25) consists of filters and an active amplifier with output CM regulation. The class D output is filtered by the linear resistor and capacitor (RC) filter formed by R_1 and C_S. The RC filter bandwidth is set high enough to ensure loop stability. Shunt resistors (R_S) are added to attenuate the filtered class D signal to a level that can be easily accommodated by the active feedback amplifier (A). The attenuation factor from the shunt resistor (R_S) is compensated by adjusting the value of resistor R_{FDBK}. The R and C around the amplifier provide additional filtering.

Fabricated in a commercial 180-nm CMOS process, the die photo is shown in Figure 26. The top right is the feedforward path. The feedback filter path is at the bottom left, and the predriver with source resistors is at the middle. The die measures 1.5 mm × 1.3 mm. The class D amplifier together with the integrated power management unit is packaged in a low-cost wire-bonded package. The class D amplifier is measured with an 8-Ω resistor in series with a 68-µH inductor while other power management units are operating. The 68-µH

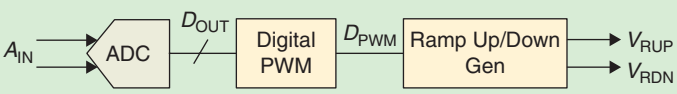

FIGURE 24: A feedforward ADC path.

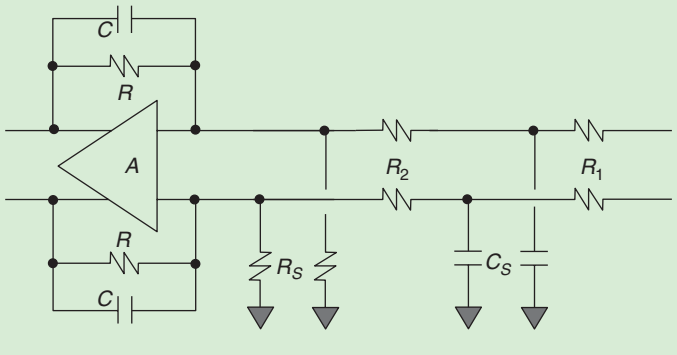

FIGURE 25: A feedback filter path.

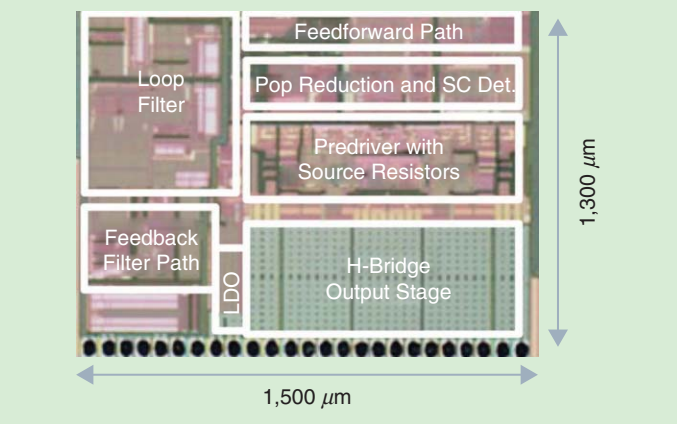

FIGURE 26: A die microphotograph.

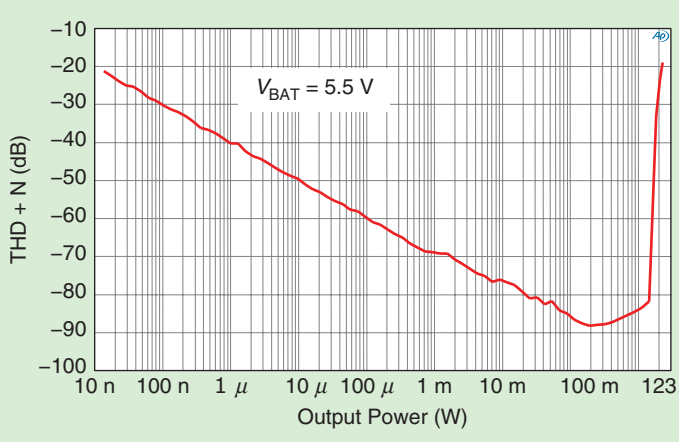

FIGURE 27: Measured THD+N versus output power.

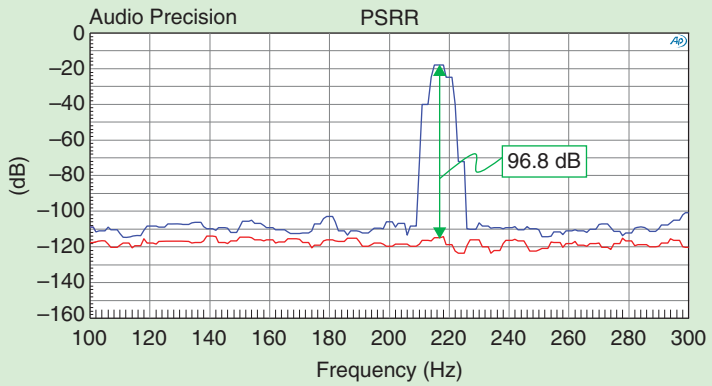

FIGURE 28: Measured PSRR.

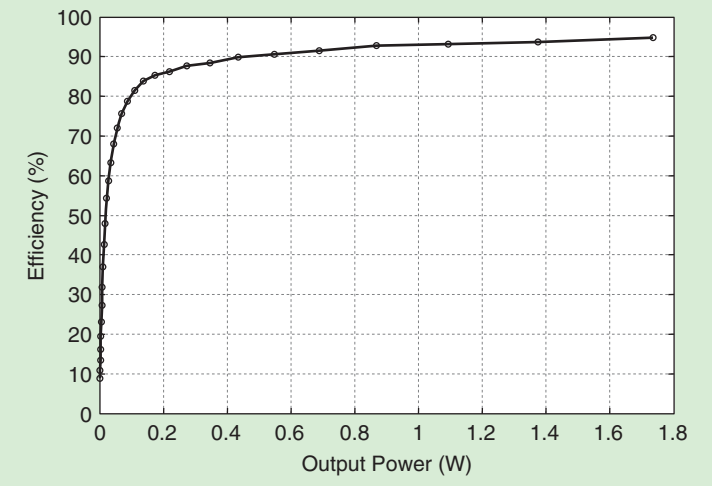

FIGURE 29: Measured class D efficiency.

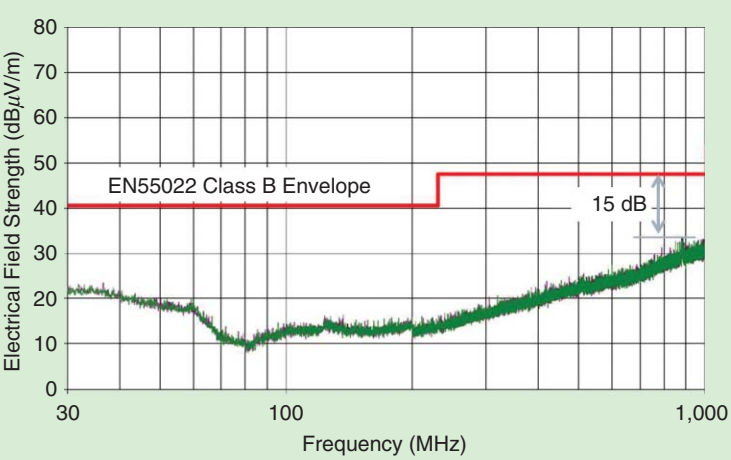

FIGURE 30: Measured radiated emission.

inductor and the 8-Ω resistor are used to emulate the 8-Ω loudspeaker. The design supports battery voltages from 2.5 to 5.5 V. Figure 27 shows a plot of the A-weighted THD+N with a 1-kHz input signal using audio precision equipment. The signal-to-noise ratio (SNR) is calculated by adding 60 dB to the absolute value of the THD+N at –60 dBFS. The class D amplifier achieves over 105 dB SNR when driving an 8-Ω loudspeaker. The minimum THD+N is 0.004%. At –40 dB THD+N, the output power corresponds to 1.75 W. The power supply rejection is measured with a 400 mV_{PP} disturbance on the battery supply and a –60 dBFS input signal.

Figure 28 shows the measured spectrum of both the supply and the class D amplifier output. A PSR of 96.8 dB is achieved at the GSM time division multiple access frequency of 217 Hz. The class D efficiency versus output power is shown in Figure 29. A peak efficiency of 95% is achieved at a 1.75-W power output. The radiated electromagnetic emission was measured with a commercial smartphone that uses this class D amplifier. The measured class D radiation is shown in Figure 30. Edge-rate control enables the system to meet the is European emission standard EN55022 class B standard with a 15-dB margin. The EN55022 class B standard is more stringent compared to North American standards. The class D amplifier pop-and-click noise level was measured with an audio precision analyzer, with A-weighted filtering applied to emphasize the frequency range over which the human ear is sensitive. For a class D amplifier with a 4-V achievable output voltage level, the amplifier pop-click-noise level was reduced from 27 mV, shown at the top of Figure 31 with pop-and-click suppression disabled, to 1 mV with the suppression circuit enabled, as shown at the bottom.

In summary, compared to other amplifier classes such as AB, G, and H, class D has superior efficiency. Audio class D amplifiers can be realized using digital PWM architecture and analog feedback

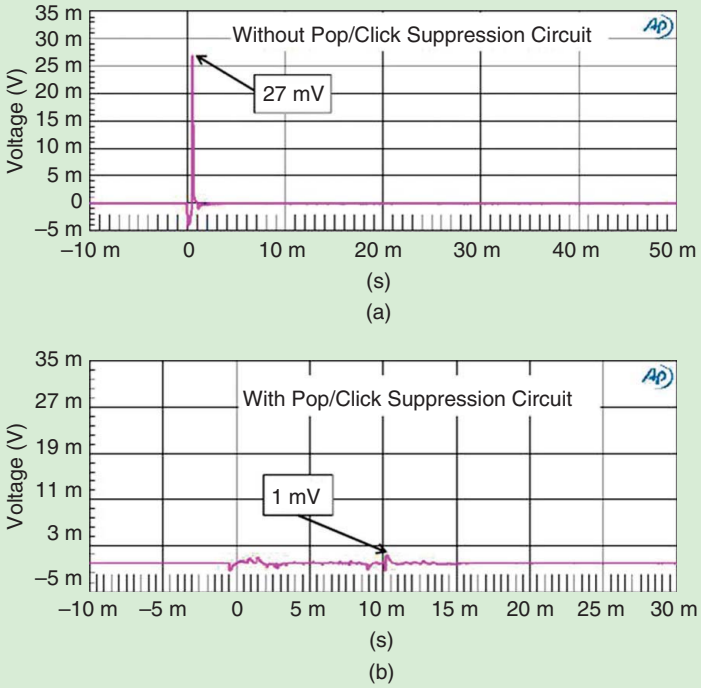

FIGURE 31: A class D pop/click performance.

PWM architecture. An enhanced analog feedback PWM class D amplifier with a wire bond package achieves 95% peak efficiency and a 105-dB dynamic range. The feedforward ADC path and edge-rate control enables a high output power and high margin for EMC. The feedback filter path enables the 0.004% minimum THD+N performance. And the fourth-order loop filter helps to achieve 96-dB PSRR. A 1-mV pop/click is achieved with auxiliary loop and ramp up/down techniques.

Acknowledgments

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SSC

Christian Enz, Francesco Chicco, and Alessandro Pezzotta

Nanoscale MOSFET Modeling

Part 1: The simplified EKV model for the design of low-power analog circuits

This article presents the simplified charge-based Enz–Krummenacher–Vittoz (EKV) [11] metal–oxide–semiconductor field-effect transistor (MOSFET) model and shows that it can be used for advanced complementary metal–oxide–semiconductor (CMOS) processes despite its very few parameters. The concept of an inversion coefficient (*IC*) is first introduced as an essential design parameter that replaces the overdrive voltage $V_G - V_{T0}$ and spans the entire range of operating points from weak via moderate to strong inversion (SI), including the effect of velocity saturation (VS). The simplified model in saturation is then presented and validated for different 40- and 28-nm bulk CMOS processes. A very simple expression of the normalized transconductance in saturation, valid from weak to SI and requiring only the VS parameter λ_c, is described. The normalized transconductance efficiency G_m/I_D, which is a key figure-of-merit (FoM) for the design of low-power analog circuits, is then derived as a function of *IC* including the effect of VS. It is then successfully validated from weak to SI with data measured on a 40-nm and two 28-nm bulk CMOS processes. It is then shown that the normalized output conductance G_{ds}/I_D follows a similar dependence with *IC* than the normalized G_m/I_D characteristic but with different parameters accounting for drain induced barrier lowering (DIBL). The methodology for extracting the few parameters from the measured $I_D - V_G$ and $I_D - V_D$ characteristics is then detailed. Finally, it is shown that the simplified EKV model can also be used for a fully depleted silicon on insulator (FDSOI) and FinFET 28-nm processes.

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Introduction

With its stringent requirements on the energy consumption of electronic

devices, the Internet of Things has become the primary driver for the design of low-power analog and radio-frequency (RF) circuits [1]. The implementation of increasingly complex functions under highly constrained power and area budgets, while circumventing the challenges posed by modern device technologies, makes the analog/RF design exercise ever more challenging. The designer often needs to make optimum choices to achieve the required gain, current efficiency, bandwidth, linearity, and noise performance [2], [3].

To this purpose, he often starts his new design using simple transistor models to explore the design space and identify the region offering the best tradeoff before fine-tuning his design by running more accurate simulations using the full fetched compact model available in the design kit [4], [5]. This task has been made more difficult in advanced CMOS technologies due to the down-scaling of CMOS processes and the reduction of the supply voltage, which has progressively pushed the operating point from the traditional SI region toward moderate (MI) and even weak inversion (WI), where the simple quadratic model is obviously no more valid [6], [7]. This has led to an increased interest in the concept of *IC* as the main design parameter replacing the overdrive voltage even for advanced technologies [8], [9].

This article presents the simplified EKV transistor model in saturation since, except for switches, most transistors in CMOS analog circuits are biased in saturation. The article is split in two parts: the first part introduces the simplified EKV model in saturation and shows that it can be used even for advanced bulk CMOS technologies. The second part of the article, to be published in an upcoming issue of *IEEE Solid-State Circuits Magazine*, will show how the inversion coefficient can be used as the main design parameter to describe various FoMs to explore basic tradeoffs faced in analog and RF design.

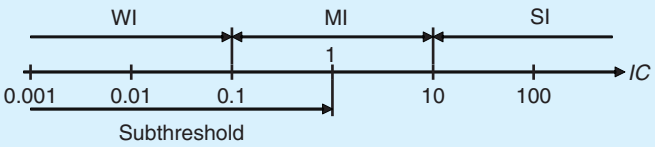

FIGURE 1: The different regions of operation in terms of the inversion coefficient.

The Concept of Inversion Coefficient

Definition

The *inversion coefficient IC* is a measure of the inversion level in the channel of a single MOSFET and is defined as [10]

$$IC \triangleq \frac{I_D}{I_{\text{spec}}}\Big|_{\text{saturation}}, \tag{1}$$

where the normalizing factor I_{spec} is called the *specific current* and is defined as [10]

$$I_{\text{spec}} \triangleq I_{\text{spec}\square} \cdot \frac{W}{L} \quad \text{with}$$
$$I_{\text{spec}\square} \triangleq 2n\mu_0 C_{ox} U_T^2, \tag{2}$$

where W and L are the width and length of the transistor, n is the slope factor, μ_0 is the low field mobility in the channel region, C_{ox} the oxide capacitance per unit area, and $U_T \triangleq kT/q$ is the thermodynamic voltage. In a given technology, the specific currents per square $I_{\text{spec}\square}$, one for each transistor type (n- and p-channel), are the most fundamental parameters for the designer.

Using *IC*, the different regions of operation of a MOSFET can be classified as illustrated in Figure 1 and defined as

$$\begin{aligned} &IC \leq 0.1 \text{ WI}, \\ &0.1 < IC \leq 10 \text{ MI}, \\ &10 < IC \text{ SI}. \end{aligned} \tag{3}$$

The specific current has originally been defined in [11] using the normalized $G_m nU_T/I_D$ characteristic as discussed in the section "The Transconductance Efficiency G_m/I_D." It corresponds to the drain current for which the long-channel SI asymptote $1/\sqrt{IC}$ crosses the WI asymptote, which turns out to be equal to unity as shown in Figure 2.

The specific current I_{spec} can actually be extracted for a given technology and transistor type using the circuit shown in Figure 3 [12], [13]. This circuit is based on the Vittoz current reference represented by transistors M1–M4, where the original resistor is replaced by M6 [14]. M1 and M2 are biased in WI and saturation, whereas M6 and M7 in SI (M6 in the linear region and M7 in saturation). Assuming that $A \gg 1$, it

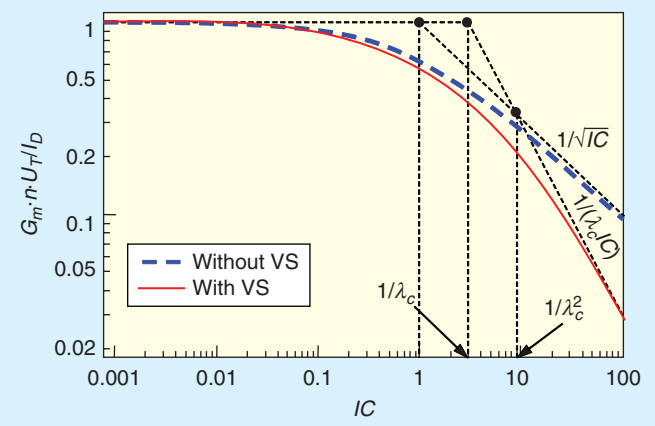

FIGURE 2: g_{ms}/i_d versus *IC* showing the long- and short-channel asymptotes.

The designer often needs to make optimum choices to achieve the required gain, current efficiency, bandwidth, linearity, and noise performance.

can be shown that the bias current I_b is proportional to I_{spec6} and I_{spec7}

$$I_b = I_{spec6} \cdot A \cdot ln^2(K) = I_{spec7} \cdot ln^2(K), \quad (4)$$

where $K \triangleq \beta_2/\beta_1$ with $\beta_i = \mu_0 C_{ox} W_i / L_i$ for $i = 1, 2$. This circuit allows the inversion coefficient of any n-channel transistor to be precisely set independently of the value of the threshold voltage from the reference transistor. Indeed, any n-channel transistor Mx can be operated at a given inversion factor IC_x by means of a weighted copy of current I_b. For a transistor Mx that has to be biased in WI, it is best to use transistor M1 as a reference transistor whereas M7 should be used as reference transistor for biasing a transistor in SI. The drain current of transistor Mx is then N times the bias current $I_x = N \cdot I_b$ and hence $IC_x \cdot W_x/L_x = N \cdot IC_1 \cdot W_1/L_1$. The aspect ratio W_x/L_x of transistor Mx is then given by

$$\frac{W_x}{L_x} = N \cdot \frac{IC_1}{IC_x} \cdot \frac{W_1}{L_1}. \quad (5)$$

This circuit is therefore ideal for migrating circuits from one technology to another with a minimum of redesign. Note that another current reference is needed for extracting the specific current for p-channel transistors.

The Simplified EKV MOSFET Model

The Large-Signal dc Model

The drain current in saturation normalized to the specific current, which actually corresponds to IC defined earlier, is given by [15], [16]

$$IC = \frac{4(q_s^2 + q_s)}{2 + \lambda_c + \sqrt{4(1+\lambda_c) + \lambda_c^2 (1+2q_s)^2}}, \quad (6)$$

where q_s is the normalized inversion charge $q_i \triangleq Q_i/Q_{spec}$ taken at the source with $Q_{spec} \triangleq -2nU_T C_{ox}$ [10]. Parameter λ_c is accounting for VS according to

$$\lambda_c \triangleq \frac{L_{sat}}{L} \quad (7)$$

and scales inversely proportional to the transistor length L. λ_c actually corresponds to the fraction of the channel in which the carrier drift velocity reaches the saturated velocity v_{sat} over a portion of the channel length L_{sat} defined as

$$L_{sat} = \frac{2\mu_0 U_T}{v_{sat}}. \quad (8)$$

The normalized source charge q_s is related to the terminal voltages by [10]

$$\frac{V_P - V_S}{U_T} = 2q_s + ln(q_s), \quad (9)$$

where $V_P - V_S$ is the saturation voltage for a long-channel transistor (i.e., without VS), $V_P \cong (V_G - V_{T0})/n$ is the pinch-off voltage, and V_S is the source-to-bulk voltage. Note that, in the EKV model, all the terminal voltages are referred to the local substrate instead of the source terminal to preserve the symmetry of the device in the model [10].

The normalized saturation voltage can be expressed in terms of the inversion coefficient IC by solving (6) for q_s leading to

$$q_s = \frac{1}{2} \cdot \left(\sqrt{4IC + (1 + \lambda_c \cdot IC)^2} - 1 \right) \quad (10)$$

and using (10) in (9). Unfortunately, (9) cannot be inverted to express IC in terms of $V_P - V_S$ and hence of the terminal voltages.

This simplified charge-based model only requires four parameters to fit the $I_D - V_G$ transfer characteristic: the slope factor n, the specific current per square $I_{spec\square}$, the threshold voltage V_{T0}, and the VS parameter L_{sat}. The methodology to extract these parameters from measured data is explained in the section "Parameter Extraction." Typical values for these parameters for a 28-nm bulk CMOS process are given in Table 1.

The I_D versus $V_G - V_{T0}$ transfer characteristics are plotted in Figure 4

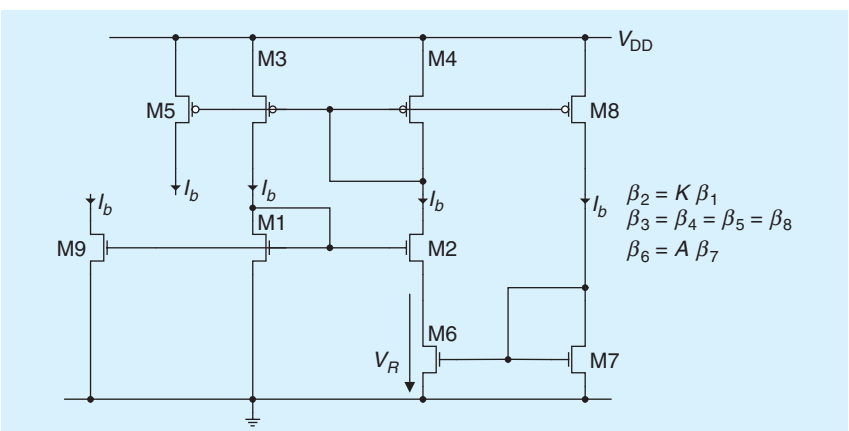

FIGURE 3: The current reference for extracting the specific current for n-channel transistors [12]–[14].

TABLE 1. TYPICAL PARAMETER VALUES FOR A 28-nm PROCESS.

	n	$I_{spec\square}$ [nA]	V_{T0} [V]	L_{sat} [nm]
n-channel	1.1–1.5	850	0.4–0.55	15–25
p-channel	1.1–1.5	350	0.35–0.5	15–25

and compared to measurements made on wide and minimal length transistors from three different processes, a 40-nm and two different 28-nm bulk CMOS processes. Although the drain current is measured from sweeping the gate voltage, the simplified EKV model is calculated from the measured current by first normalizing it to the specific current for each transistor to get the inversion coefficients, from which the overdrive voltages are computed using (10) and (9). Despite the very few number of parameters, the simple model fits the measurements very well over more than six decades of current. Note that the extraction of the parameters $I_{spec\square}$ and L_{sat} is done for several different geometries (in particular, different length) illustrating the rather good scalability of the simplified model. Notice that the measured points and analytical models of the $W = 108\ \mu m, L = 30\ nm$ (red circles) and $W = 108\ \mu m, L = 40\ nm$ (green squares) transistors almost fall on top of each other, indicating that the normalization almost completely strips off the technology dependence. The difference with the $W = 3\ \mu m, L = 30\ nm$ (blue diamonds) characteristic is due to a slightly larger value of λ_c. In other words, the four parameters almost fully characterize the technology at least for the transfer characteristics in saturation and in the regions of operation used for analog circuit design.

The large-signal output characteristic in the saturation region has always been the most difficult part to model due to a combination of several effects including VS, channel length modulation (CLM) and DIBL. Figure 5 shows the inversion coefficient versus the drain voltage for different overdrive voltages measured on a large and minimal length transistor from a 28-nm process. It shows that the current can be approximated in saturation by a simple linear characteristics

$$I_D \cong G_{ds} \cdot (V_D + V_M), \qquad (11)$$

where V_M is the CLM (or Early) voltage and G_{ds} is the output conductance that corresponds to the slope

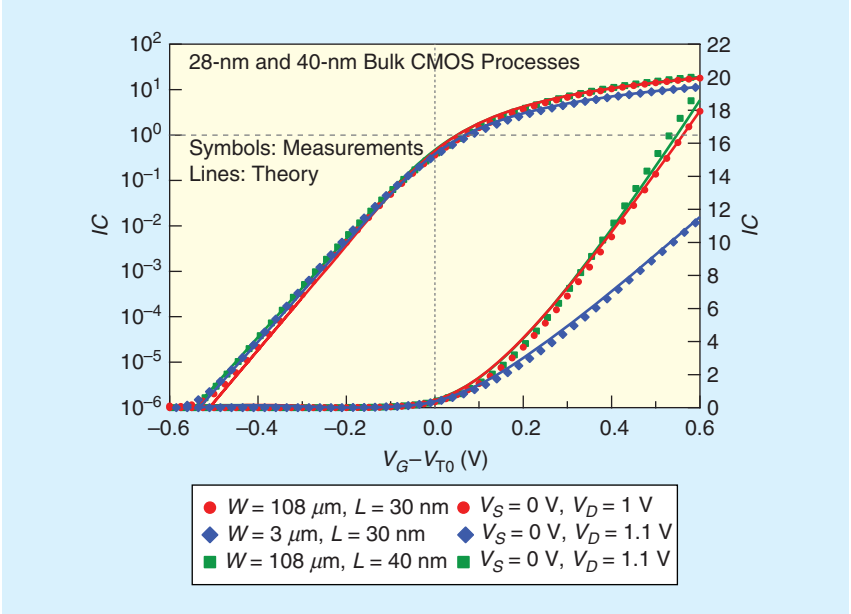

FIGURE 4: *IC* versus the overdrive voltage $V_G - V_{T0}$ measured in saturation on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.

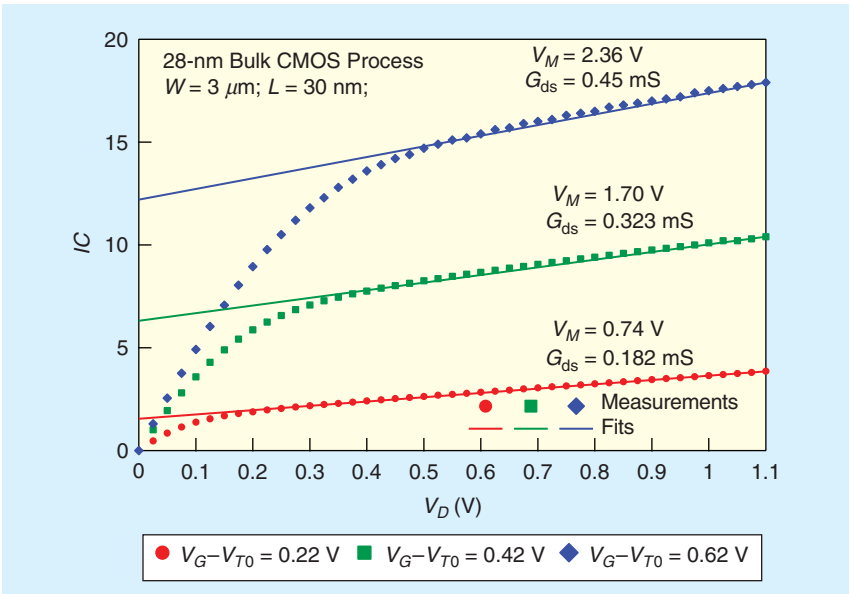

FIGURE 5: *IC* versus V_D measured for different overdrive voltages on a minimum length transistor 30-nm from a 28-nm bulk CMOS processes.

and is discussed further in the next section. (Note that even though the parameter V_M is called the CLM voltage, it actually embeds all of the effects, including VS and DIBL, which is actually dominant in WI.)

The Small-Signal dc Model

The most important small-signal parameter is without doubt the gate transconductance G_m. Since in the EKV model the voltages are all referred to the bulk, we can define two other transconductances: the source transconductance $G_{ms} \triangleq -\partial I_D/\partial V_S$ and the drain transconductance $G_{md} \triangleq \partial I_D/\partial V_D$ [10]. Note that G_{md} should not be confused with the output conductance G_{ds}. In saturation $G_{md} = 0$ and $G_{ms} = n \cdot G_m$.

The transconductance efficiency, sometimes also called the current efficiency, is one of the most important FoMs for low-power analog circuit design.

The normalized source transconductance in saturation g_{ms} can be expressed in terms of IC as [4], [15]

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n \cdot G_m}{G_{spec}} = \frac{\sqrt{(\lambda_c IC+1)^2+4IC}-1}{\lambda_c(\lambda_c IC+1)+2}, \quad (12)$$

where $G_{spec} \triangleq I_{spec}/U_T = 2n\mu_0 C_{ox} U_T$. g_{ms} is plotted versus IC in Figure 6 and favorably compares to measurements obtained from the derivative of the characteristics shown in Figure 4 over a very wide range of bias (more than four decades of current). Note that for short-channel devices in SI, the $I_D - V_G$ transfer characteristic becomes a linear function of the gate voltage as illustrated in Figure 4 and, hence, the gate transconductance becomes independent of the drain current and of the gate length L. It then only depends on W and v_{sat} according to

$$g_{ms} \cong 1/\lambda_c \text{ for } IC \gg 1 \text{ or } G_m \cong WC_{ox}v_{sat}. \quad (13)$$

The inverse of the VS parameter λ_c is therefore a key parameter since it gives the maximum normalized transconductance that can be achieved for a short-channel device in a given technology.

The other key dc small-signal parameter is the output conductance G_{ds} which, together with the transconductance, defines the intrinsic (or self) gain G_m/G_{ds}. As mentioned previously, the output conductance is the result of several physical effects including VS, CLM, and DIBL. In advanced short-channel devices biased in MI or WI, DIBL is the dominant effect. The latter is defined as the variation of the threshold voltage with respect to the applied drain-to-source voltage, i.e., $\partial V_T/\partial V_{DS}$ and can be modeled as [17]–[19]

$$V_T \cong V_{T0} \cdot (1 - \sigma_d \cdot V_{DS}), \quad (14)$$

where the parameter $\sigma_d \triangleq \partial V_T/\partial V_{DS}$ accounts for DIBL and depends on L and V_S [18], [19]. The output conductance can then be written as [20]

$$G_{ds} \triangleq \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{DS}} = \sigma_d \cdot G_m, \quad (15)$$

where $\partial I_D/\partial V_T = -G_m$ has been used. A model of the output conductance versus IC can now be derived using the expression of $G_m = G_{ms}/n$ in saturation given in (12), where λ_c is replaced by an additional parameter λ_d

$$g_{ds} \triangleq \frac{G_{ds}}{G_{spec}} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{\lambda_d(\lambda_d IC+1)+2}. \quad (16)$$

The normalized output conductance versus IC given by (16) is plotted in Figure 7 and compared to measurements made on a long and short transistor from a 28-nm CMOS process. Figure 7 shows that the model fits very well the measured data over more than five decades of current despite its simplicity.

The Transconductance Efficiency G_m/I_D

The transconductance efficiency G_m/I_D, sometimes also called the *current efficiency*, is one of the most important FoMs for low-power analog circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of IC. As will be shown in the second part of this article, the transconductance efficiency (or its inverse) appears in many expressions related to the optimization of analog circuits. In normalized form, the transconductance efficiency is defined as the actual transconductance obtained at a given IC with respect to the maximum transconductance $G_m = I_D/(nU_T)$ reached in WI [4], [15]

$$\frac{g_{ms}}{IC} = \frac{G_m \cdot nU_T}{I_D} = \frac{\sqrt{(\lambda_c IC+1)^2+4IC}-1}{IC \cdot [\lambda_c(\lambda_c IC+1)+2]}. \quad (17)$$

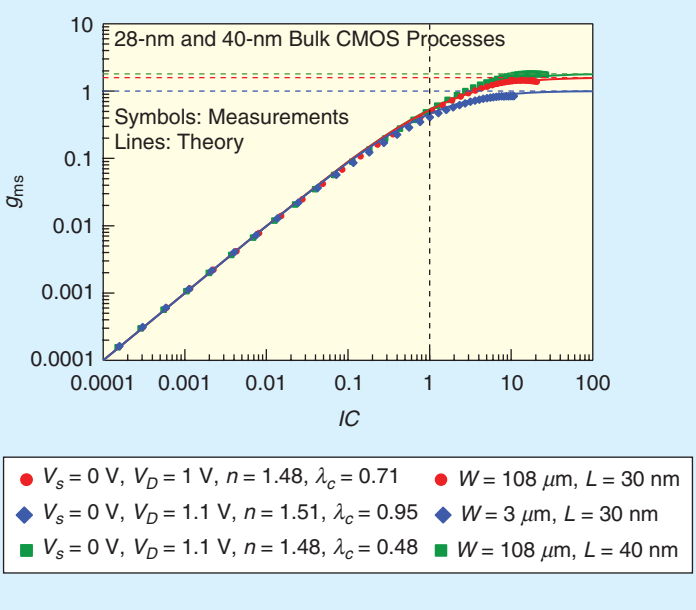

FIGURE 6: Normalized transconductance g_{ms} versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.

The expression in (17), which is continuous from WI to SI and includes the effect of VS, is plotted in Figure 2. The figure shows that $G_m nU_T/I_D$ is maximum in WI and decreases as $1/\sqrt{IC}$ in SI for long-channel devices in which VS is absent (dashed blue curve). Note that the specific current has been defined from the $G_m nU_T/I_D$ versus I_D characteristic of a long-channel transistor as the current at which the WI and SI asymptotes cross. This is why these two asymptotes cross at $IC = 1$ when $G_m nU_T/I_D$ is plotted versus IC as in Figure 2.

As shown in Figure 4, for short-channel devices subject to VS, the drain current in SI becomes a linear function of the gate voltage, independent of the transistor length. Hence, the transconductance becomes independent of the current and length. Since G_m becomes independent of I_D, and hence of IC, the $G_m nU_T/I_D$ curve scales like $1/(\lambda_c IC)$ in SI (red curve) instead of $1/\sqrt{IC}$ when VS is absent. In essence, the effect of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to obtain the same transconductance than without VS. Nevertheless, irrespective of the channel length, $G_m nU_T/I_D$ remains invariant (i.e. $g_{ms}/IC = 1$) in WI, since short-channel effects (SCEs), including VS, have the same effect on G_m than on I_D simply because G_m is proportional to I_D in WI. As shown in Figure 2, the inversion coefficient for which the SI asymptote of a short-channel device crosses the horizontal unity line is equal to $1/\lambda_c$. As discussed in the next section, this is how the parameter λ_c is extracted from measurements on a short-channel device.

The normalized transconductance efficiency given by (17) is compared to measurements in Figure 8 for the same devices as shown in Figures 4 and 6. Despite that the normalized $G_m nU_T/I_D$ only requires one parameter (λ_c or L_{sat}), the model fits very well to the data over more than five decades of IC.

In a similar way, we can define the G_{ds}/I_D ratio, which from (11) turns out

This article presents the simplified EKV transistor model in saturation since, except for switches, most transistors in CMOS analog circuits are biased in saturation.

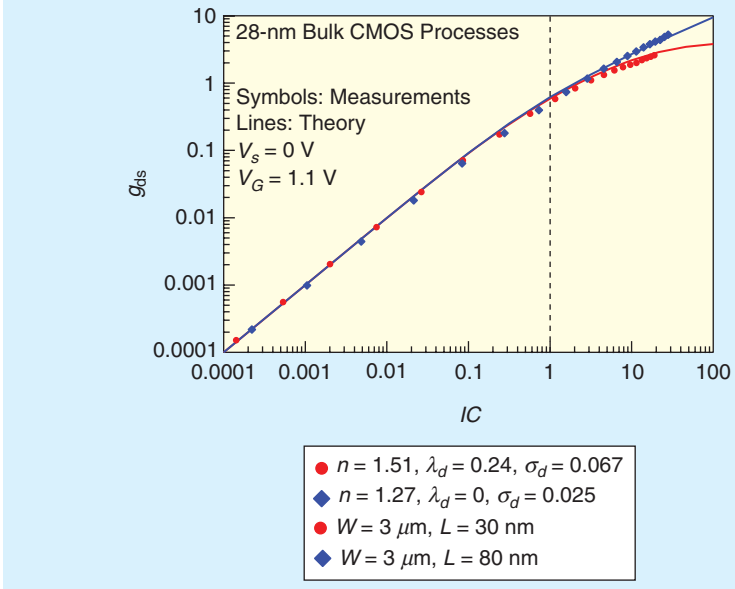

FIGURE 7: Normalized output conductance g_{ds} versus IC measured on minimum and medium length transistors from a 28-nm bulk CMOS process.

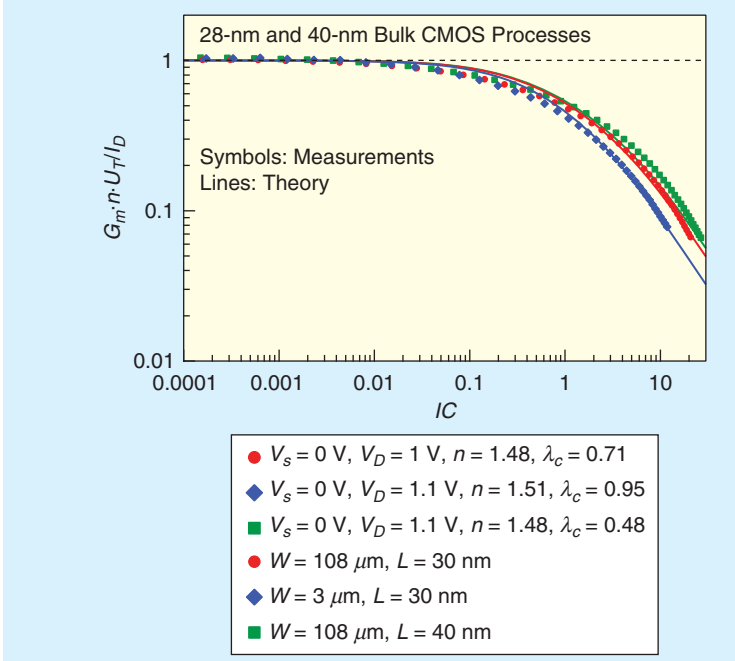

FIGURE 8: Normalized transconductance efficiency g_{ms}/IC versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.

The most important small-signal parameter is without doubt the gate transconductance G_m.

to be about equal to $1/V_M$ for $V_D \ll V_M$. In normalized form, we have

$$\frac{U_T}{V_M} \cong \frac{G_{ds} U_T}{I_D} = \frac{g_{ds}}{IC} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{IC\cdot[\lambda_d(\lambda_d IC+1)+2]}. \quad (18)$$

From (18), we can deduce that the highest output conductance for a given current is reached in WI and is equal to $G_{ds\text{-}max} \triangleq \sigma_d I_D/(nU_T)$. We can then normalize the output conductance to $G_{ds\text{-}max}$ for the normalized output conductance to reach unity in WI

$$\frac{G_{ds}}{G_{ds\text{-}max}} = \frac{n}{\sigma_d} \cdot \frac{g_{ds}}{IC} = \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{IC\cdot[\lambda_d(\lambda_d IC+1)+2]}. \quad (19)$$

Equation (19) is plotted in Figure 9 and compared to measurements made on the same transistors than in Figure 7 and shows good agreement with the measured data. Note that, unlike for the transconductance, where we want to get the highest transconductance for a given current reached in WI, the output conductance should be minimized for a given current. It will be shown in Part 2 of this article that, even though the output conductance decreases in SI, the self-gain remains actually maximum in WI and simply equal to $1/\sigma_d$.

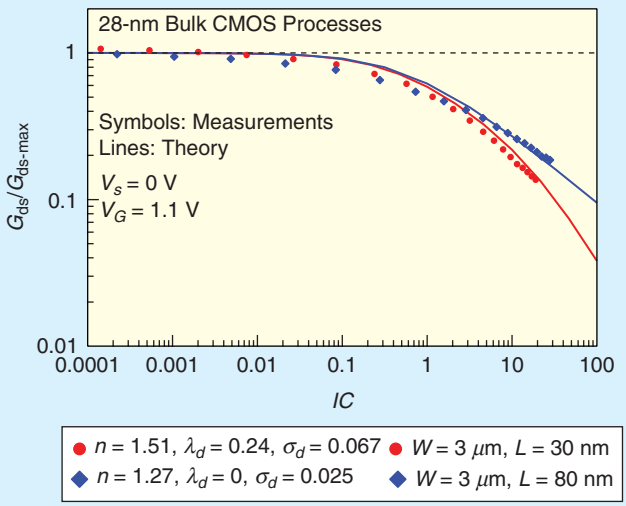

FIGURE 9: Output conductance-to-current ratio $G_{ds}/G_{ds\text{-}max}$ versus IC measured on minimum and medium length transistors from a 28-nm bulk CMOS process.

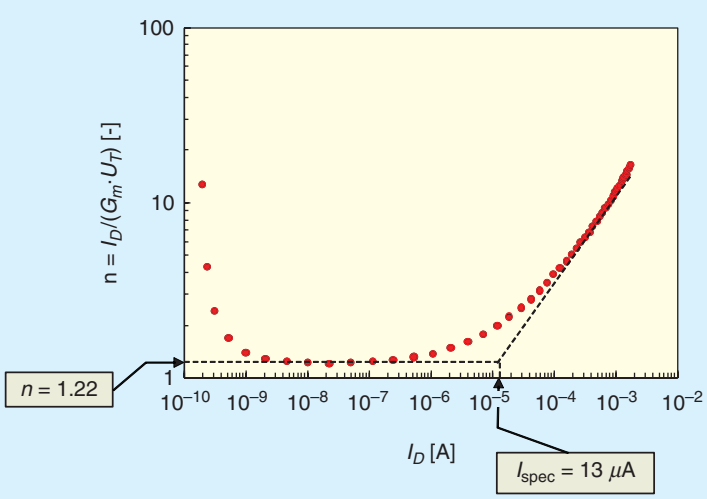

FIGURE 10: The extraction of the slope factor n and the specific current I_{spec}.

Parameter Extraction

The four parameters n, I_{spec}, V_{T0}, and L_{sat} required for fitting the simplified model described in the section "The Large-Signal dc Model" to measured $I_D - V_G$ data can be extracted from measurements following the procedure described below. The extraction starts from the $I_D - V_G$ characteristic measured on a wide and long transistor. After calculating (or measuring) the derivative G_m, the slope factor n is extracted from the plateau reached by the $I_D/(G_m U_T)$ curve in WI as in Figure 10. The specific current for this particular device is then obtained by the intersection between the SI asymptote $\propto \sqrt{I_D}$ and the slope factor horizontal line as shown in Figure 10. For this particular long-channel device, this results in $n = 1.22$ and $I_{spec} = 13\,\mu A$, from which we can derive the specific current per square $I_{spec\square}$ by dividing by the aspect ratio W/L.

The VS parameter λ_c is extracted in Figure 11 from the normalized $G_m n U_T/I_D$ characteristic of a wide and short-channel transistor as the IC corresponding to the intersection of the $1/IC$ asymptote with the unity horizontal line after having properly extracted the slope factor n, which is usually affected by SCEs ($n = 1.48$ in this case compared

to $n = 1.22$ as extracted from the long-channel device). This results in $\lambda_c = 0.48$ and hence $L_{sat} = 19.5$ nm for this particular 40-nm transistor.

Finally, the threshold voltage is extracted from the $I_D - V_G$ characteristic to fit the measured data as shown in Figure 4.

The DIBL parameter σ_d used for the output conductance can be extracted in a similar way than the slope factor n by looking at the plateau of the normalized $G_{ds}nU_T/I_D$ curve reached in WI, while the λ_d parameter can be extracted in a similar way than the VS parameter λ_c from the normalized $G_{ds}/G_{ds\text{-}max}$ given by (19) for a short transistor.

Simplified Model Applied to FDSOI and FinFET

Although the simplified model described here was developed for transistors fabricated in a bulk CMOS process, it can also be used for transistors fabricated in an FDSOI process. However, it doesn't model the effect of the additional back gate available in FDSOI processes, and the extracted parameters would be valid only for a single back gate voltage. An example of IC versus $V_G - V_{T0}$ and $G_m nU_T/I_D$ versus IC measured on three different transistor lengths from a 28-nm FDSOI process are shown in Figure 12. Except for some deviation observed on the $G_m nU_T/I_D$ versus IC at high IC values, which is probably due to additional mobility reduction due to vertical field, the match between the model and the measured characteristics is surprisingly good.

The model was even tried with transistors coming from a 28-nm

This article presents the simplified EKV model in saturation and shows that it can successfully model the large- and small-signal behavior over a wide range of bias.

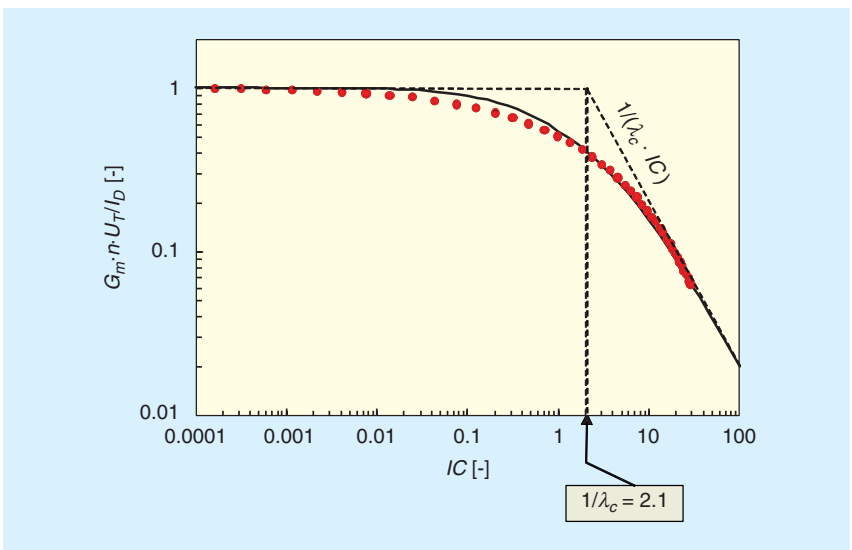

FIGURE 11: The extraction of λ_c on a short device.

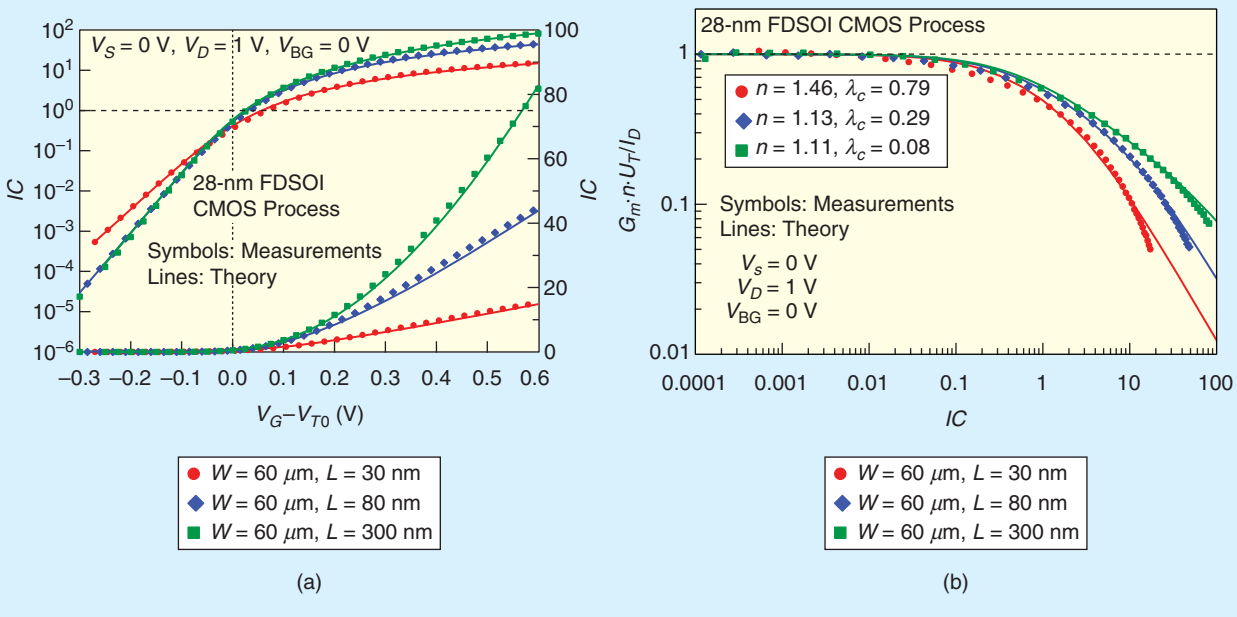

FIGURE 12: The simplified EKV model applied to a 28-nm FDSOI CMOS process. (a) IC versus $V_G - V_{T0}$ and (b) $G_m nU_T/I_D$ versus IC for three different transistor lengths.

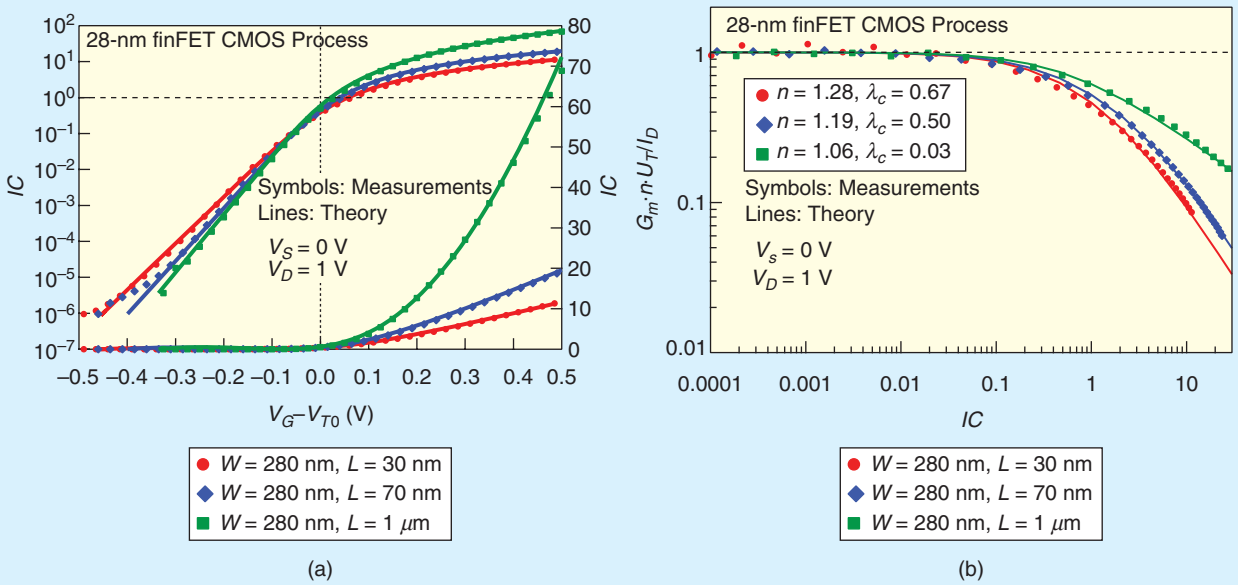

FIGURE 13: The simplified EKV model applied to a 28-nm FinFET CMOS process. (a) IC versus $V_G - V_{T0}$ and (b) $G_m nU_T/I_D$ versus IC for three different transistor lengths.

FinFET process. Figure 13 shows the IC versus $V_G - V_{T0}$ and $G_m nU_T/I_D$ versus IC measured on three different transistor lengths. Again, after proper parameter extraction, the model fits the measured data very well, despite its simplicity.

Conclusions

Analog designers usually like to use simple analytical transistor models to help them identify the optimum bias region in the overall design space where they can pick an initial point close to the optimum target by setting the bias and choosing the transistor size. Further optimization can then be conducted using circuit simulators with the full fetched compact model available in the design kit. Because of the down-scaling of the supply voltage inherent to advanced CMOS technologies, the operating points are pushed more and more toward moderate and even WI, where the standard quadratic model obviously doesn't hold anymore. A simple transistor model valid in all regions of operation from WI to SI is therefore required. This article presents the simplified EKV model in saturation and shows that, despite the very few number of parameters, it can successfully model the large- and small-signal behavior over a wide range of bias.

The concept of inversion coefficient IC is first introduced to replace the overdrive voltage as the main design parameter covering the whole range of operating points from WI to SI across MI. IC is defined as the ratio of the drain current in saturation to the specific current I_{spec}. The latter is proportional to W/L and to the specific current per square $I_{spec\square}$, which is the most important process parameter for the analog designer. It is shown that the specific current can be extracted using a current reference circuit that provides a bias current that allows the inversion coefficient of a given transistor to be precisely set. This bias technique is limited by the transistor matching but is completely independent of the threshold voltage and its variations.

The simplified EKV charge-based model in saturation is then presented, and the $I_D - V_G$ transfer characteristic is validated for different 40- and 28-nm bulk CMOS processes. A very simple expression of the normalized transconductance versus IC is given requiring only a single parameter, the VS parameter λ_c. It is shown that the maximum normalized transconductance reached by a short-channel transistor in SI is simply equal to $1/\lambda_c$. The normalized transconductance efficiency $G_m nU_T/I_D$, which is a key FoM for the design of low-power analog circuit, is then derived as a function of IC. It is shown that the $G_m nU_T/I_D$ characteristic of a short-channel transistor in SI decreases as $1/(\lambda_c IC)$ instead of $1/\sqrt{IC}$ for a long-channel transistor. This means that, because of VS, more current is required to reach the desired transconductance for a short-channel device compared to the ideal case where VS would be absent. Despite that it requires only the VS parameter λ_c, the $G_m nU_T/I_D$ versus IC fits the measured data from 40- and 28-nm bulk CMOS processes extremely well over a large range of bias.

It is then shown that the normalized output conductance $G_{ds}U_T/I_D$

follows the same dependence than the normalized $G_m nU_T/I_D$ characteristic, but with a different parameter λ_d replacing λ_c and an additional parameter σ_d accounting for the effect of DIBL. How to extract all the required parameters from the $I_D - V_G$ and $I_D - V_D$ characteristics measured in saturation on a long- and a short-channel device is presented. Finally, it is concluded that the simplified EKV model can also be used for transistors from a FDSOI and FinFET 28-nm processes.

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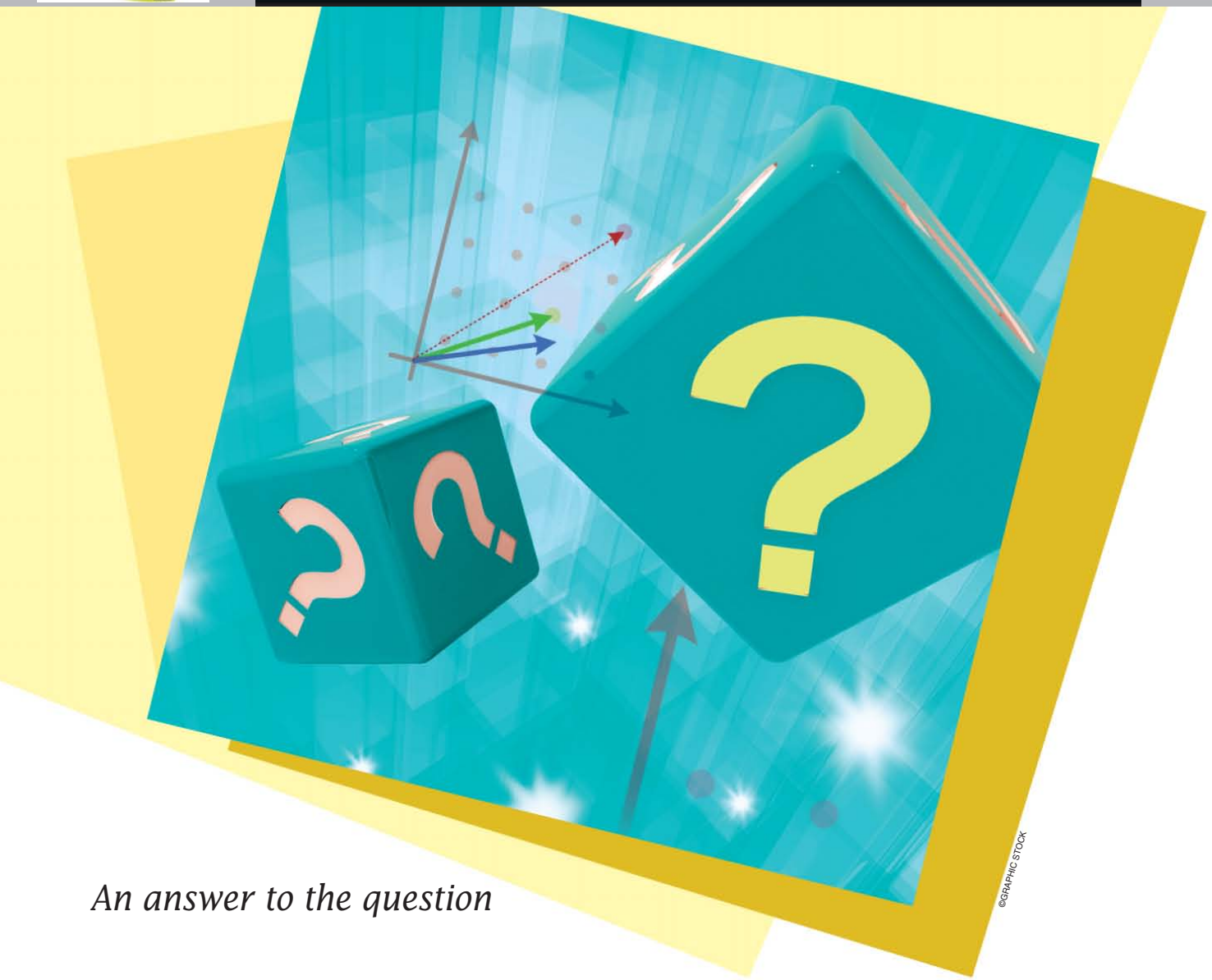

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An answer to the question

To EVM or Two EVMs?

Marco Vigilante, Earl McCune, and Patrick Reynaert

Error vector magnitude (EVM) is a key indicator of modulated signal quality. It measures how far a transmitted or received constellation point is from its ideal location.

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Compared to other system-level specifications such as bit error rate, the EVM contains more information about amplitude and phase distortion and circuit limitations. It is designed to be a measurement of in-band signal quality. This is one of the major reasons why EVM is widely used to quantify the degradation of modulated signals due to circuit impairments, especially for transmitters and including the effects from power amplifiers (PAs). However, there are multiple ways to calculate EVM, and these methods do not provide identical results. Therefore, it is important to be aware of these differences when a comparison with the state of the art is made. For any performance comparison to be valid, it is essential to apply the exact same

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metric. Otherwise, the comparison is not valid.

Within a specific communication standard, the method to measure or calculate EVM is clearly indicated; but when no standard is available, one must be careful. This is especially true for 5G—the fifth generation of wireless systems—which as of this writing does not yet have a standard.

To better understand the different ways to calculate EVM, it is useful to briefly go back to its definition. Figure 1 shows the normalized first-quadrant constellation diagram for a 64-quadrature amplitude modulation (QAM) signal. At the optimal sampling point, one calculates the error vector as the difference between the measured and ideal symbol. This error vector is represented by a complex number based at the ideal constellation point. The EVM is now defined as a ratio of the root mean square (RMS) value of all the error vectors, averaged over N symbols, and then divided by *some normalization factor* [see (1)]. The calculation is done over many symbols N to avoid the influence of bit pattern segments. The number of symbols N needs to be large enough to ensure that all possible symbols and transitions are observed.

Two EVM definitions are commonly used [1], [2]. The first one is a ratio of RMS magnitudes,

$$\mathrm{EVM_{RMS}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} |S_{\mathrm{ideal},i} - S_{\mathrm{meas},i}|^2}}{\sqrt{\frac{1}{M}\sum_{i=1}^{M} |S_{\mathrm{ideal},i}|^2}} = \frac{V_{\mathrm{error,RMS}}}{C_{\mathrm{RMS}}}, \quad (1)$$

where C_{RMS} is the RMS value of the constellation point magnitudes. The second compares the RMS magnitude of the errors to the peak magnitude of the constellation,

$$\mathrm{EVM_{max}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} |S_{\mathrm{ideal},i} - S_{\mathrm{meas},i}|^2}}{|S_{\mathrm{max}}|} = \frac{V_{\mathrm{error,RMS}}}{C_{\mathrm{max}}}, \quad (2)$$

Compared to other system-level specifications such as bit error rate, the EVM contains more information about amplitude and phase distortion and circuit limitations.

where $S_{\mathrm{ideal},i}$, $S_{\mathrm{meas},i}$, and S_{max} are defined for the ith symbol in Figure 1. $\mathrm{EVM_{RMS}}$ normalizes the RMS value of the error vectors to the RMS level of the M-ary signal constellation, while $\mathrm{EVM_{max}}$ adopts the maximum constellation magnitude as its normalization factor [1]. The two definitions coincide for constellations with constant magnitude [e.g., quadrature phase shift keying (QPSK), binary PSK, and 8PSK] while $\mathrm{EVM_{RMS}} > \mathrm{EVM_{max}}$ for constellations with multiple possible magnitudes (e.g., amplitude PSK, Star-QAM, 16-QAM, and 32-QAM). It should be noted that, based on the authors' measurement experiences, Keysight uses $\mathrm{EVM_{max}}$ as a default setting whereas Rohde & Schwarz uses $\mathrm{EVM_{RMS}}$ as default in its measurement setup. As such, this already leads to some confusion when comparing measurement results.

There also is a third EVM metric to add to this confusion: $\mathrm{EVM_{peak}}$ is the maximum value of the error vector magnitude that has occurred over sets of N symbols each. One must be particularly careful not to confuse $\mathrm{EVM_{max}}$ with $\mathrm{EVM_{peak}}$.

From (1) and (2), it is evident that the difference between $\mathrm{EVM_{RMS}}$ and $\mathrm{EVM_{max}}$ has something to do with the peak-to-average power ratio (PAPR) of the signal. However, the difference between $\mathrm{EVM_{RMS}}$ and $\mathrm{EVM_{max}}$ is—maybe surprisingly—not equal to the PAPR of the radio frequency (RF) signal. Indeed, the difference between the two is equal to the PAPR of the ideal constellation diagram, i.e., before any Nyquist or channel filtering takes place. The PAPR of the constellation diagram itself can easily be calculated [3], and some numbers for well-known modulation formats are shown in Table 1. When the baseband filtering is applied, the PAPR of the signal increases above the PAPR of the constellation itself. For the examples in Table 1, this PAPR increase is 4 dB for a typical square-root-raised cosine filter with α equal to 0.35.

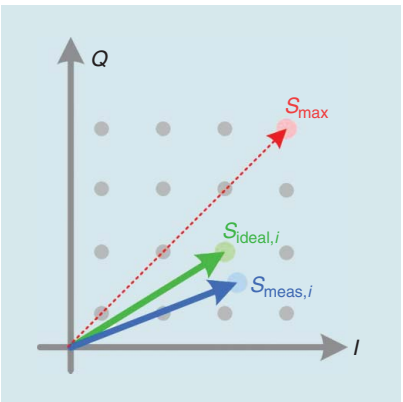

FIGURE 1: A normalized constellation diagram for 64-QAM. Only the first quadrant is shown for simplicity.

TABLE 1. AN OVERVIEW OF CONSTELLATION PAPR AND SIGNAL PAPR NUMBERS FOR FIVE DIFFERENT CONSTELLATION DIAGRAMS.

CONSTELLATION DIAGRAM	QPSK	8PSK	16-QAM	64-QAM	256-QAM
PAPR of the ideal constellation	0 dB	0 dB	2.6 dB	3.7 dB	4.2 dB
PAPR of the RF signal after square-root-raised-cosine filter (α = 0.35)	4 dB	4 dB	6.6 dB	7.7 dB	8.2 dB
PAPR increase from filtering	4 dB	4 dB	4 dB	4 dB	4 dB

There are multiple ways to calculate EVM, and these methods do not provide identical results.

Now that we touched upon PAPR, this gives us the opportunity to address another point of confusion among electrical engineers with different backgrounds. There is a key difference in the definition for PAPR for analog and RF designers. The PAPR for an analog signal is equal to the peak instantaneous power divided by the average power of the signal. Crest factor is another metric used by analog designers and is defined as the peak voltage over the RMS voltage of the signal. Therefore, PAPR is the square of crest factor. But for RF designers, the PAPR of a modulated carrier is defined differently. It is equal to the peak-envelope power (PEP) divided by the RMS power of the signal. PEP is the average power of a sinewave having an amplitude equal to the peak instantaneous voltage of the modulated carrier. Therefore, from an RF perspective, an unmodulated carrier has a PAPR of one (or 0 dB), whereas that same signal has a PAPR of two (or 3 dB) for an analog designer. This is to be expected, since a baseband amplifier (operational transconductance amplifier or op-amp) needs excellent circuit linearity to properly amplify a sinusoidal signal with constant envelope, while a bandpass RF PA does not require any circuit linearity to achieve the very same goal (see switch-mode PAs [4]). Therefore, it is strongly suggested to use the term crest factor for broadband analog circuits and PAPR for RF circuits. In any case, one should realize that PAPR has a different definition for analog and RF!

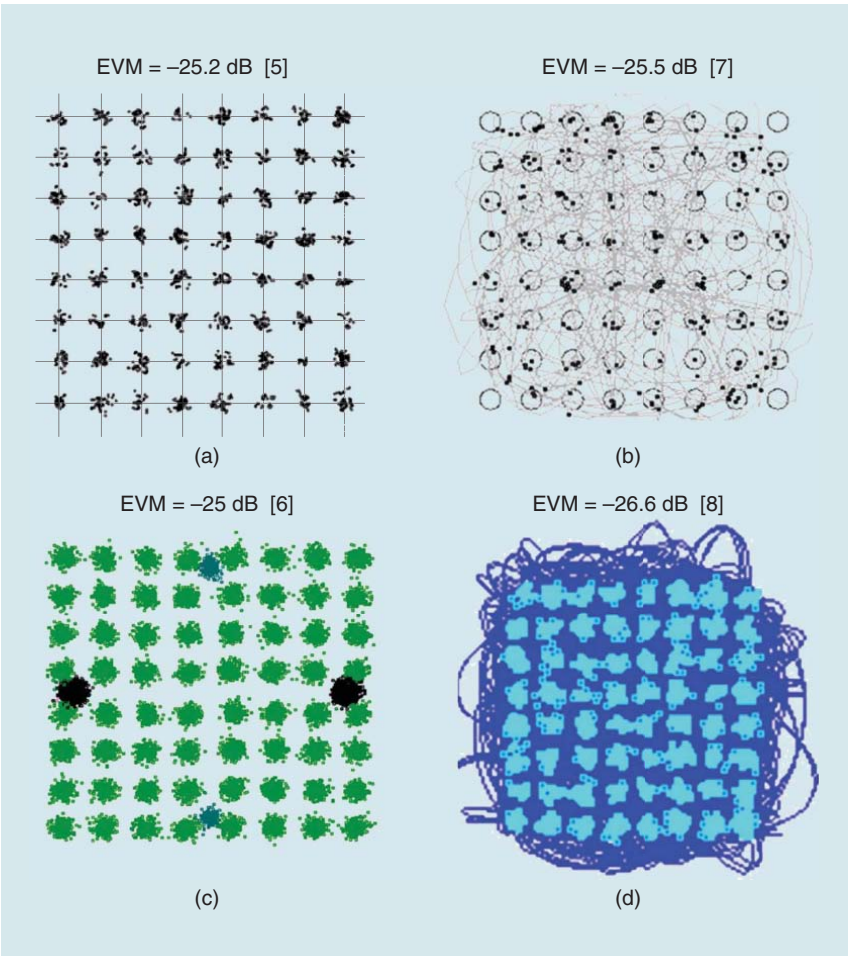

FIGURE 2: Measured constellation and reported EVM of four state-of-the-art mm-wave PAs for future 5G presented at the IEEE International Solid-State Circuits Conference in recent years [5]–[8]. Note that (b) has no points at the constellation corners, clearly showing circuit compression, which is not seen in the other measurements (yet the same EVM value is reported).

With the background developed so far, it is easy to derive $EVM_{RMS} \approx EVM_{max} + 2.6$ dB for 16-QAM, $EVM_{RMS} \approx EVM_{max} + 3.7$ dB for 64-QAM, and $EVM_{RMS} \approx EVM_{max} + 4.2$ dB for 256-QAM [3]. The EVM_{RMS} metric is presently most appropriate to compare the signal quality for different modulation schemes. And in the presence of additive white Gaussian noise only, EVM_{RMS} is equal to –SNR [2].

A good example of confusion arising from using different EVM metrics is shown in Figure 2. It shows four different measured constellation plots and the reported EVM of four state-of-the-art mm-wave PAs developed for future 5G communications [5]–[8]. All of them amplify a 64-QAM modulated signal, provide measured results, use a published definition of EVM, and appear to achieve similar benchmark EVM numbers (all are around –25 dB). But clearly, for the same reported –25-dB EVM, the constellation plots look quite different. Indeed, the definition of EVM used in [5] and [6] is EVM_{RMS}, whereas the one used in [7], [8] is EVM_{max}. It is worth noting that any PA design entails a stringent tradeoff between efficiency and linearity. The requirements on output signal accuracy are often set by an EVM metric. To put things in perspective, a –25-dB EVM allows a 3-dB margin on the required SNR for a 64-QAM signal [5] when using EVM_{RMS}. This margin disappears if the EVM_{max} metric is used. To meet the specifications, a substantial power back-off from the maximum achievable output power is needed, compromising efficiency. Therefore, a ≈3.7-dB difference in the EVM

definition immediately results in a very misleading comparison table, especially if the normalization used is omitted. Unfortunately, several comparison tables of this kind can be found to date in the literature. Therefore, while we wait for the 5G standard to be released, it is important to clearly indicate the equation that is used to calculate EVM.

Well, that last argument is valid even after the 5G standard is put into place …

While we wait for the 5G standard to be released, it is important to clearly indicate the equation that is used to calculate EVM.

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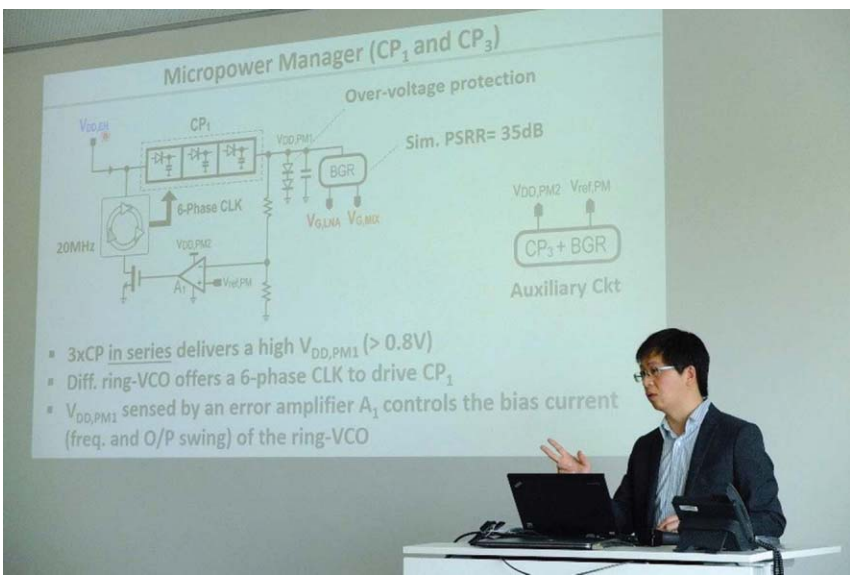
CHAPTERS

DL Prof. Pui-In Mak Gives a Technical Talk Hosted by imec in Leuven, Belgium

The IEEE Solid-State Circuits Society (SSCS) Benelux Chapter organized a technical talk on 23 May 2017 given by Pui-In (Elvis) Mak, associate director of research and associate professor, State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, China. Mak is an SSCS Distinguished Lecturer (DL); the program is aimed at disseminating high-quality technical content to members at a local level.

In his talk, "Ultra-Low-Power Radios Using Current-Reuse/Function-Reuse/Ultra-Low-Voltage Techniques," Mak discussed the work his research group is doing in Macau, where over 80 researchers focus on analog and mixed-signal ICs for wireless communications, data converters, biomedical and power electronics, and analytical chemistry. He then positioned his work compared to the state of the art on low-power radio transceivers, where his group targets 10x lower power than existing solutions, for comparable battery life times. In this light, he explored several techniques that led to numerous publications in the International Solid-State Circuits Conference as well as *IEEE Journal of Solid-State Circuits*.

Mak explained how transistors can be stacked to reuse quiescent currents, even when only low supplies are



Prof. Mak discusses techniques for low-power receiver ICs.

imec, Leuven, Belgium, hosted this SSCS Benelux DL technical talk, which was well received by an audience from industry and academy.

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available. He shared a prototype design that reuses the functionality of a voltage-controlled oscillator (VCO) that directly drives an off-chip load, de-facto functioning as the power amplifier. The design innovatively uses a six-port transformer that cross-couples the VCO structure and provides differential-to-single ended conversion as well as conjugate power matching in a compact form factor and includes a digital PLL for amplitude-constant signal modulation. He detailed these techniques as exemplified in a low-power Bluetooth, low-energy receiver chip implemented in a 28-nm CMOS and a ZigBee receiver chip implemented in 65-nm CMOS.

For this event, imec hosted more than 20 members at its location in Leuven, Belgium. The audience consisted of students, researchers, and industry engineers. Mak's talk was well received, as illustrated by various interactive questions during the Q&A session.

—Piet Wambacq
Barend van Liempd
SSCS Benelux Chapter

SSCS American University of Sharjah Student Branch Chapter Recognized as Top Chapter

The IEEE Solid-State Circuits Society (SSCS) American University of Sharjah Student Branch Chapter, located in the United Arab Emirates, has been recognized as a top Student Chapter in Region 8. This award is presented annually to qualifying Student Branches in each IEEE Region. To qualify for the award, the Student Branch must conform to IEEE bylaws, have an active program, and support IEEE goals. The Chapter was officially formed in January 2016. Since then, it has held a number of activities, which are outlined next.

Wireless Technology (Wi-Tech) Symposium

The Chapter's very first activity was assisting Chapter Advisor Dr. Lutfi Albasha, chair of the Wi-Tech Symposium, with set-up, registration, and coordination. Chapter members were available at the registration stand throughout the two-day event and assisted guests by providing directions, preparing conference badges, and completing registration payments.

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Students hard at work on their electronic circuit boards.

Battle of the Engineers Competition

In collaboration with the American University of Sharjah Student Council, the Student Branch Chapter participated in the Battle of the Engineers, a competition in which engineering students of various disciplines compete to complete one challenge under each major. The Student Chapter represented the Electrical Engineering Chapter by designing an intimidating network of resistors connected in parallel and series. Students were tasked to simplify the network, in the shortest time possible, and pick out the equivalent resistance configuration from a pile of resistors.

Build-Your-Own Radio Transmitter Workshop

This was the Chapter's largest event in the fall of 2016, in collaboration with FabLab UAE. Students were invited to showcase their fundamental electronic

Some of the SSCS American University of Sharjah Student Chapter Branch members and advisors.

The SSCS American University of Sharjah held a recruiting event to inform students of the benefits of being an SSCS member.

engineering skills to build what was, for many, their first electronic printed circuit board. Upon instructing the students and aiding them when handling the soldering equipment, the students spent three hours working and testing their boards. Four hours later, they started transmitting their laughing voices, received on their mobile phones from different rooms.

This Student Branch Chapter continuously works to recruit new members and has run two recruitment day events, including one in collaboration with the IEEE Student Chapter at the American University of Sharjah. The Chapter has 164 student members.

"The Chapter is run with the initiative of contributing to the development of well-rounded engineers through their undergraduate course of study," said Chapter Chair Omar Al Aryani. "When the Chapter first started, our Chapter Advisor Dr. Lutfi Albasha expressed his desire to see students enhance their skills beyond what they learn in class." The Chapter continuously works to better student's presentation, teamwork, and communication skills.

"Fresh graduates shouldn't only be good at designing low-pass filters, but they should be able to work in teams and to express their ideas effectively," said Al Aryani.

The Chapter's officers are

- Omar Al Aryani: chair
- Fares Al Mabrouk: vice chair
- Aaesha AlZaabi: executive secretary
- Alia AlMutawa: treasurer
- Armaghan Cheema: media coordinator
- Yamen Hatahet and Ahmed Hassan: electrical engineering representatives
- Misbah Al Khadem: public relations officer.

—Abira Sengupta

Record Industry Turnout for RF Circuit and System Lecture

Over 50 students, researchers, and design engineers attended the lecture "RF Circuit and System Innovations for a New Generation of Wireless Terminals," by IEEE Solid-State Circuits Society (SSCS) Distinguished Lecturer Prof. Peter Kinget from Columbia University, New York. The lecture was held at the Tyndall National Institute, Cork, Ireland, on 29 March 2017 (http://www.tyndall.ie/).

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In addition to local academic participants from Tyndall National Institute, University College Cork, Cork Institute of Technology, and the Microelectronic Circuit Centre Ireland (MCCI), the lecture attracted design engineers from a record number of companies, including Altratech, Analog Devices, Arralis, Ferfics, Intel, MACOM, Qualcomm, S3 Group, Smart RF Design, ublox, and Xilinx.

Prof. Kinget discussed innovations in field-programmable receiver front ends and explained novel switched-capacitor techniques, compressed sampling, and efficient spectrum scanning solutions. This was followed by a lively discussion about trends in wireless communications.

The event was cosponsored by MCCI (http://www.mcci.ie) and Science Foundation Ireland's CONNECT Centre for Future Networks and Communications (http://www.connectcentre.ie/).

—Peter Kennedy
Chair, United Kingdom and Ireland Chapter

NICOLA COONEY, MCCI

Peter Kinget (front row, sixth from left) and colleagues at Tyndall National Institute.

SSCS Beijing Chapter Hosts Dr. Jerald Yoo

Dr. Jerald Yoo, National University of Singapore, visited the IEEE Solid-State Circuits Society Beijing Chapter to present "Design Strategies for Wearable Sensor Interface Circuits—From Electrodes to Signal Processing." The lecture was held on 18 May 2017 at the campus of Tsinghua University, Beijing, China. Approximately 40 graduate students from local universities and research institutes and four faculty members attended the event. The lecture was of particular interest to researchers and students who are interested in the area of biomedical IC design. Attendees had a very interesting discussion with Yoo about biopotential signal readout

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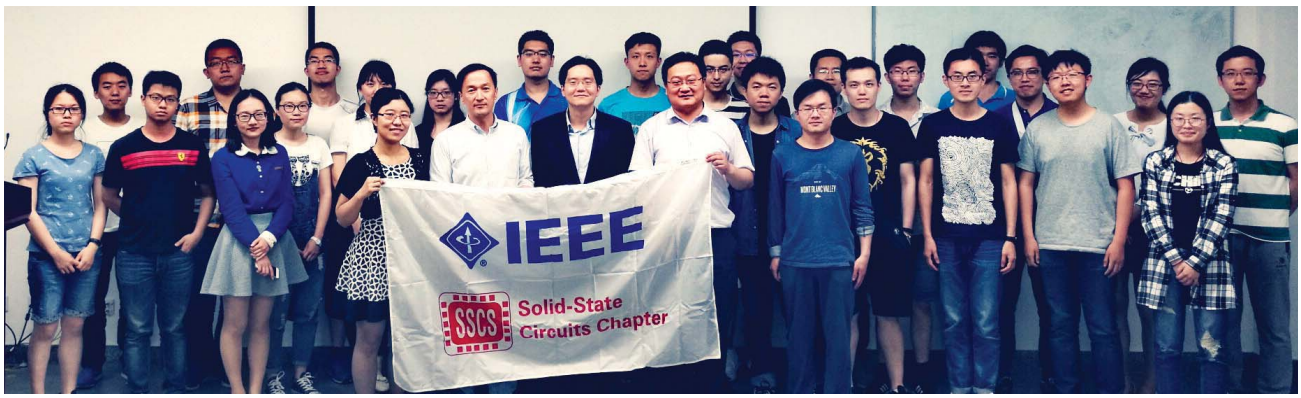

The attendees, Chapter officers, and Jerald Yoo at the lecture hosted by the SSCS Beijing Chapter.

circuit design and patient-specific epileptic seizure classification of system-on-a-chip design. "The seminar provided the local IC community a great opportunity to directly communicate with the top expert in state-of-the-art biomedical IC design techniques," said Hanjun Jiang, chair of the SSCS Beijing Chapter.

Abstract

Wearable health-care sensors provide attractive opportunities for the semiconductor sector. The target here is to mitigate the impact of chronic diseases by providing continuous yet adequate low-noise monitoring and analysis of physiological signals. However, the wearable environment is challenging for circuit designers due to its unstable skin-electrode interface. Wet and dry electrodes have significantly different electrical characteristics that need to be addressed. Also, the tradeoff between available resources and performance among the components, both in the analog front end and the digital back end, is crucial.

This lecture covers the design strategies of biointerface circuits for such wearable sensors. We will first explore the difficulties, limitations, and potential pitfalls in wearable interfaces and strategies to overcome such issues. After that, system-level considerations for better key metrics such as energy efficiency will be introduced. Several state-of-the-art instrumentation amplifiers that emphasize different parameters will also be discussed. We will then see how the signal analysis impacts the analog interface circuit design. The lecture will conclude with interesting aspects and opportunities that lie ahead.

—Hanjun Jiang,
Chapter Chair, SSCS Beijing

SSCS Tsinghua Student Chapter Visits ADI Beijing Office

The IEEE Solid-State Circuits Society (SSCS) Student Branch Chapter of Tsinghua University–Qing Hua organized a visit to the Beijing office of Analog Devices, Inc. (ADI). ADI is one of the leading semiconductor companies and a world leader in marketing a broad portfolio of high-performance analog, mixed-signal, and digital signal processing ICs that are used by over 100,000 customers worldwide.

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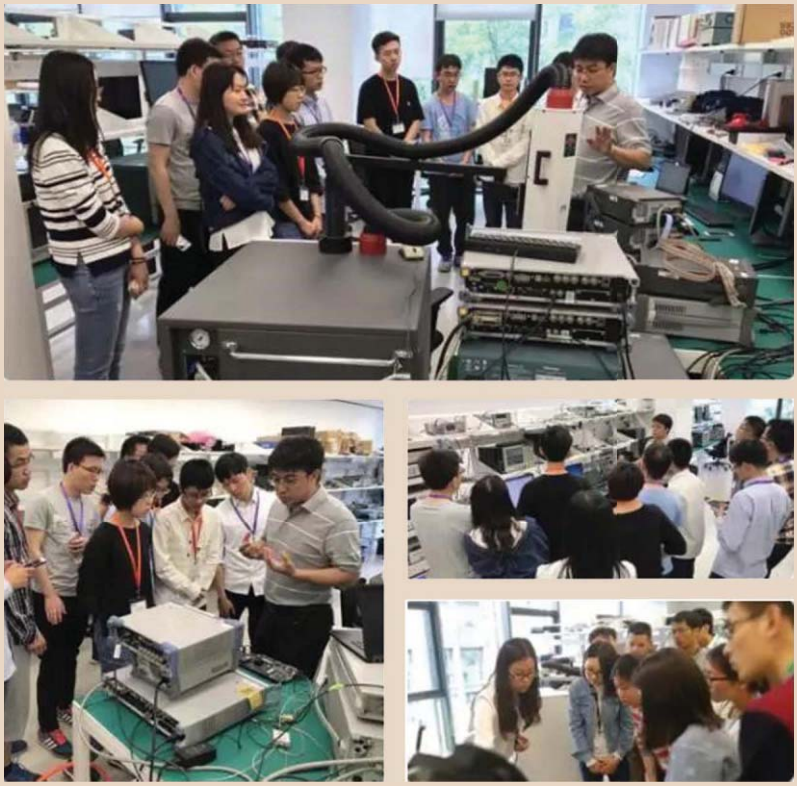
Members of the SSCS Tsinghua University Student Branch at ADI.

This visit was the first activity of the newly established SSCS Tsinghua Student Chapter. The research and development director of ADI China, Morton Zhao, welcomed the students and briefly discussed the history of the company. Zhao believed that the students, the future young engineers, would bring new views and fresh knowledge to ADI. He wanted to show the students how the company drives innovations. Bob Yang, Research and Development manager as well as a Tsinghua University alumnus, introduced the training program and career development for new employees. He also encouraged the students to apply for an internship at ADI. Yang believed this activity would be a win–win for both the students and ADI. The impression of ADI will be helpful for the students when making decisions on their first full-time jobs. Yao Zhao, an engineer who joined the company a year ago, talked about his experiences at ADI and shared the importance of picking a career that matches your interests.

After the discussion and mentoring session, the students toured the laboratory of the Research and Development center. This center developed many pieces of top-level and widely used electronic equipment. The functions of the equipment used daily were discussed.

The students took part in a teamwork-building activity that tasked them with using newspapers to build a bridge with a height higher than a water bottle to hold the weight of an apple. The group with the longest bridge won the game.

Yang gave a closing speech and talked about the tough choice between a career in industry and academia that many students will face someday.



Students participated in various activities at ADI, including learning about various types of equipment engineers use daily.

—Milin Zhang
Advisor, SSCS Tsinghua Student Chapter Branch

SSCS Benelux Chapter Holds Second Annual Chip Design Contest and Workshop

On 23 May 2017, the IEEE Solid-State Circuits Society (SSCS) Benelux Chapter organized its yearly workshop for the second time. The event was held at TU Delft, The Netherlands, hosted by Prof. Kofi Makinwa and Prof. Fabio Sebastiano from TU Delft, and attended by 29 SSCS Benelux Chapter members. The purpose of the workshop was twofold: it brought together the Benelux SSCS members around their common passion for IC design, and the winners of the 2016–2017 Chip Design Contest were awarded their prizes.

After an introduction about the Chapter by Prof. Filip Tavernier, the prizes were awarded to the three laureates: Burak Gonen (first prize, TU Delft), Bert Moons (second prize, KU Leuven), and Nicolas Butzen

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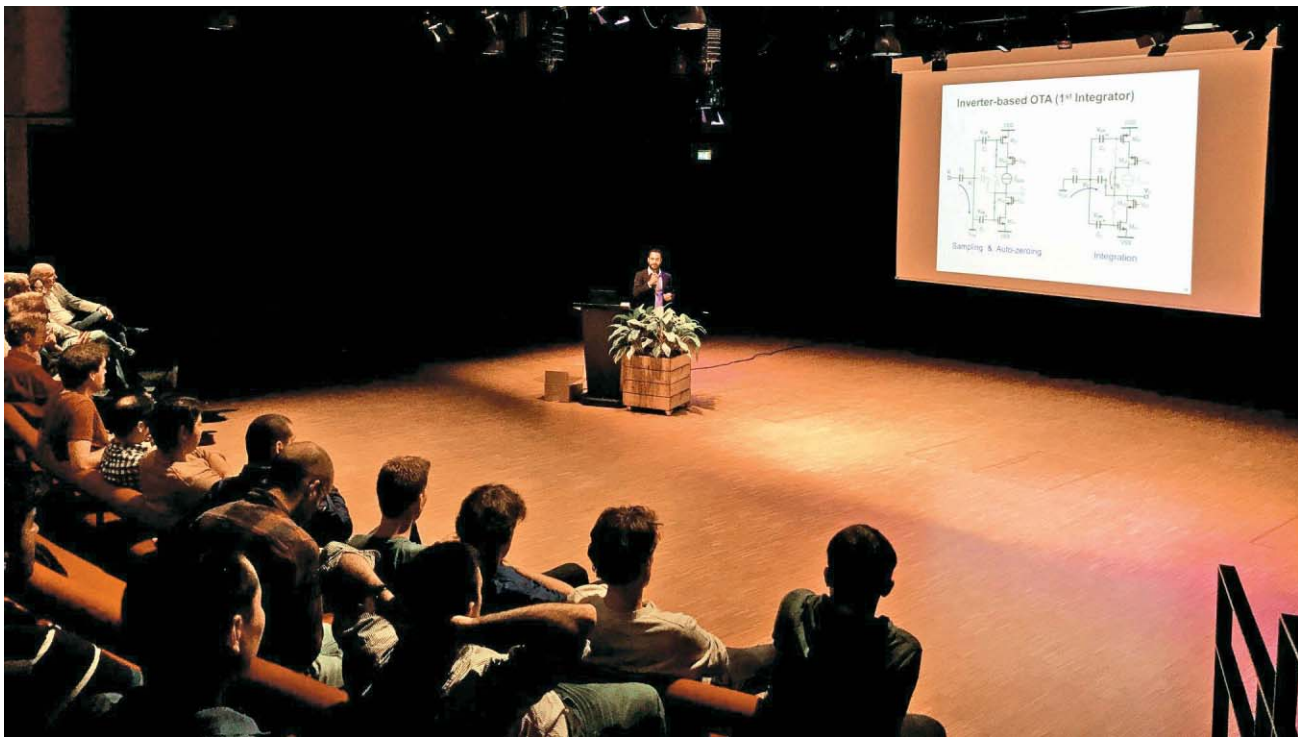


The audience listening to the talk of first-prize winner Burak Gonen.

The hosts and laureates of the Chip Design Contest (from left): Prof. Kofi Makinwa (TU Delft), Burak Gonen (TU Delft), Bert Moons (KUL), Nicolas Butzen (KUL), and Prof. Filip Tavernier (SSCS Benelux Chapter and KUL).

(third prize, KU Leuven). The workshop continued with excellent talks by the three winners about their award-winning chips. Afterward, presenter Klaas Bult gave a funny, but also confronting, talk, "Design Mistakes You Would Rather Not Talk About." The workshop concluded with a presentation by Prof. Fabio Sebastiano on Cryo-CMOS for quantum computing.

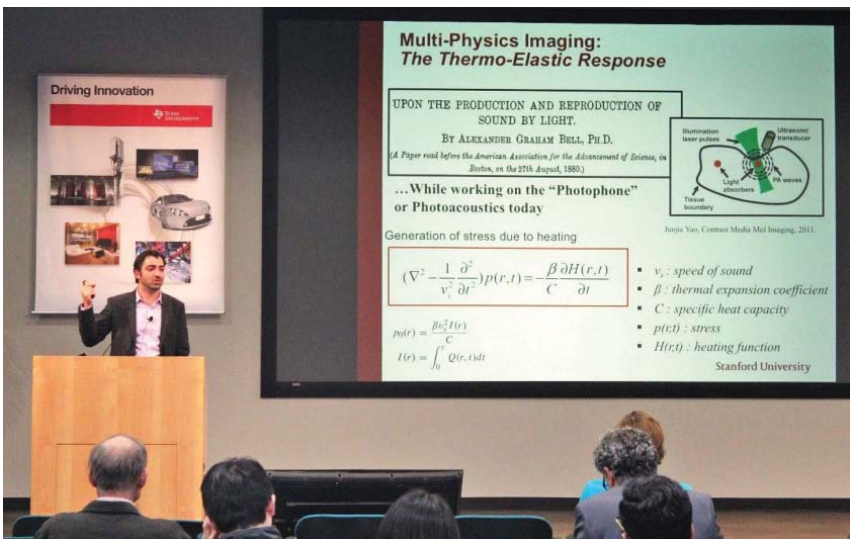
The workshop continued with excellent talks by the three winners about their award-winning chips.

During a networking reception, the participants had the opportunity to further interact while enjoying Dutch bitterballen and Grolsch, typical Dutch beers, and gave valuable suggestions to improve the impact of the workshop and the next Chip Design Contest. For the 2017–2018 academic year, the SSCS Benelux Chapter will organize a Chip Design Contest where bachelor's, master's, and Ph.D. students can participate by submitting a chip that they designed and measured.

—Patrick Reynaert
Chair, SSCS Benelux Chapter

Recent Silicon Valley SSCS Chapter Activities: Seminars, Webinars, and DL Talks

The IEEE Solid-State Circuits Society Santa Clara Valley Chapter (SCV-SSCS) held a number of seminars, webinars, and Distinguished Lecturer (DL) talks in the spring of this year. This article highlights recent events held and sponsored by the Chapter. Please feel free to contact us if you are interested in presenting at our meetings, would like to attend the Chapter events, or wish to volunteer. More information on Chapter activities and upcoming seminars is available on the Chapter website.



Prof. Amin Arbabian explaining biomedical imaging techniques at the SCV-SSCS.

SSCS webinar program speaker, Prof. Amin Arbabian, receiving the certificate of appreciation from Silicon Valley SSCS/EMBS Chapters at Texas Instruments in Santa Clara.

"On the Relationship Between Nyquist Rate and Health Care: Silicon Systems to Close the Sub-Sampling Gap in Health Screening and Monitoring"

This seminar, presented on 20 April 2017 by Prof. Amin Arbabian, Stanford University, focused on biomedical applications of silicon integrated systems in which Arbabian outlined his research on medical sensing and imaging devices that focus on increasing the sampling rate of health screening tests to approach a Nyquist rate. This Chapter had also hosted Arbabian in 2014 on a different research area, "Innovations in RF Systems," on Internet-of-Everything applications. These RF systems include mm-wave Tb/s links, radar imaging and gesture detection, mm-wave arrays/systems, medical imaging with microwave signals, and various wireless sensors.

The talk began with an overview of fundamental health-care problems including unsustainable cost trajectories and poor outcomes for a variety of disease states due to a lack of access to frequent monitoring. The introduction continued into the difference of precision health versus precision medicine from the Stanford medical school point of view, leading to opportunities for new technologies as possible solution.

Arbabian covered three main projects in his group with different approaches: 1) Medical Tricorder, a multiphysics approach for a new portable imaging and screening technology, 2) Screening the GI Tract, new monitoring platforms for personalized and precision screening, and 3) Electroceuticals, implantable devices for personalized closed-loop neuromodulation treatments that replace pharmaceuticals. Demo videos were included, showing real in vivo and in vitro applications in phantom and animal models. The talk concluded with a Q&A session.

This seminar attracted professionals from academia and industry in Silicon Valley and was cosponsored by the IEEE Silicon Valley Engineering in Medicine and Biology Society (EMBS).

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SSCS webinar program speaker Dr. Matt Straayer (right) receiving a certificate of appreciation from the SCV-SSCS Chapter chair at Texas Instruments in Santa Clara.

A video recording of this event will be available as an SSCS webinar to all SSCS members, and Arbabian will be available after the webinar to answer questions online. Society members will receive an e-mail later with the date and details of this event.

Abstract

Advances in health-care technologies have focused on therapeutics, interventional procedures, and diagnostics. These treatment steps have undergone significant improvements, leading to higher survival rates and enhancements in quality of life. Nevertheless, current trends are unsustainable due to inefficiency in addressing specific critical diseases and skyrocketing national health-care costs. An important example is cancer, where mortality rates have not seen major improvements, even with the tremendous technological advances in diagnostic imaging tools over the last four decades.

Preventive screening and continuous monitoring have the potential to completely change the landscape in the war against cancer and other complex disease states. Today, the human body is monitored/screened infrequently, in contrast with advanced electronic systems (many of which our community designs and ships), which are routinely and frequently monitored and calibrated. At best, patients only receive annual checkups with extremely low "resolution." How do we bring new screening and monitoring technologies closer to the patients (i.e., consumers)? This talk summarizes our work in this general space, from new directions in low-cost, portable, and semiconductor-based, RF-ultrasound hybrid tricorder imaging systems, to ultrasound-powered implantable devices that can measure, detect, and act upon local physiological changes through closed-loop neuromodulation or electroceuticals.

"Part 1: Time-Based Circuits—Not Just the Single Slope!"

As part of the SSCS webinar program, the SCV-SSCS organized a comprehensive two-part seminar series on time-based circuits. The material from these seminars will be available on the Silicon Valley Chapter website and the video recording will be broadcast as a webinar to SSCS members in early 2018. Part 1 of this seminar series was recorded on 18 May by Dr. Matt Straayer from Maxim Integrated Inc., "Time-Based Circuits—Not Just the Single Slope!" Part 2 was held on 17 August by Prof. Pavan Hanumolu from the University of Illinois, Urbana-Champaign, "Applications of Time-Based Circuits in Data Conversion, Filtering, and Control."

Straayer started his talk by presenting the benefits of time-based circuits, specifically that time-based signals translate to binary levels and process technology benefits binary signal processing through small area, low power, and high speed. This could have potential assets for many applications including frequency generation, analog-to-digital conversion, and switched-mode power using pulse-width modulation. An introduction to time-based circuits and their properties and a comparison with voltage or current domain signals followed next. Basic signal conversion from voltage and current domains (V&I) to time-domain and basic circuitry used for this conversion were discussed. V&I to frequency and time to V&I conversions and their corresponding circuitry were also presented.

Details of the time-to-digital converter (TDC) circuitry including classic linear TDC, Vernier TDC, two-step TDC, and their implementation details were covered next. The speaker concluded by discussing applications of time-based circuits in digital phase-locked loop, voltage-controlled oscillator -based analog-to-digital, and buck converters. The examples and tutorials for this section are available online at http://www.cppsim.com. A list of related references and recent publications, which were done in collaboration with Dr. Michael Perrott and Prof. Pavan Hanumolu, are also available.

Abstract

Compared to circuits utilizing voltage or current to convey analog signals, time-based circuits offer unique attributes, ranging from simple, area-efficient quantization to more complex techniques for time-based processing such as integration, interpolation, and noise shaping. Although time-based circuits are not new, the availability of fast, low-power transistors in advanced process nodes, combined with the challenges of traditional analog design techniques, has renewed interest in time as a signal domain both in academia and in industry. This talk will look at some obvious and more subtle differences between voltage and time-based circuits and discuss tradeoffs in the context of application requirements. A few advanced state-of-the-art time-based circuits will motivate the audience to consider how time-based circuits can be a useful tool for their own designs.

—Mojtaba Sharifzadeh
Chair, Santa Clara SSCS Chapter

SSCS Hong Kong Student Chapter Activities

Since November 2016, the IEEE Solid-State Circuits Society (SSCS) Hong Kong Student Chapter (HKSC) has organized and run a number of events including a Distinguished Lecture, circuit design competitions for school-aged children, a research seminar, and a social activity. These events were well attended and benefited by all who participated.

On 23 December 2016, in collaboration with the IEEE Circuits and Systems Society (CAS), the SSCS HKSC organized a Distinguished Lecture by Prof. Maysam Ghovanloo, GT-Bionics Lab, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta. His presentation was "Implantable and Wearable Microelectronic Devices to Improve Quality of Life for People with Disabilities." Approximately 65 IEEE Members attended the lecture.

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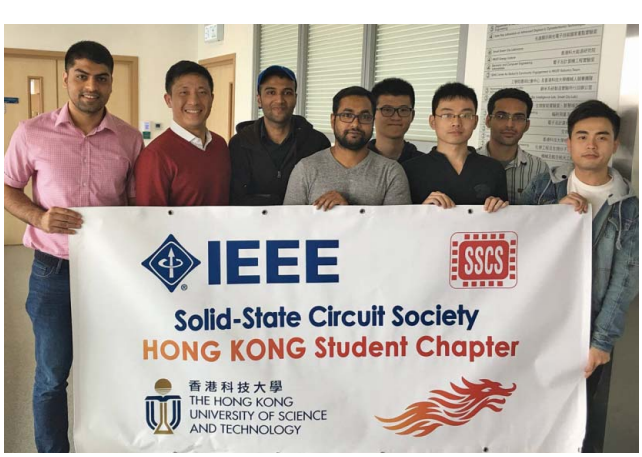
The HKSC, in collaboration with the IEEE Electronic Winter Camp, organized a three-day event for local schoolchildren, 28–30 December 2016. The event included a Hong Kong University of Science and Technology (HKUST) campus tour, lab sessions, a board game, quizzes, and lectures on number theory and randomization. This outreach program raised children's penchant for electronics.

On 13 March 2017, the Student Chapter held a membership drive to increase the number of IEEE and SSCS members at HKUST. Twenty students signed up for membership.

The IEEE SSCS HKSC committee meeting was held on 24 March 2017 to elect the Chapter chair and committee members and to discuss and plan events for the remainder of the year. Khawaja Qasim Maqbool was elected chair for the current year. Fifteen members were present at the meeting.

Along with the Hong Kong Science and Technology Parks Corporation,

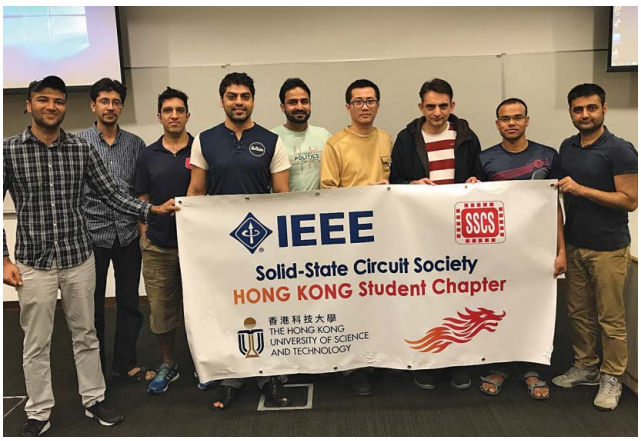
Students gathered for a Distinguished Lecture by Prof. Maysam Ghovanloo.



IEEE SSCS HKSC committee meeting attendees (from left): K.Q. Maqbool, chair; Prof. C.P. Yue, advisor; S. Raju, cochair; B. Hussain; L. Sun; G. Zhu, treasurer; M.K. Mahmoudabadi; and D. Luo, publicity head.

IEEE Electronic Endeavor Match for school kids at Hong Kong Science Park (from left): K.Q. Maqbool, chair, HKSC; Prof. M. Chan, coadvisor, HKSC; Prof. C.P. Yue, advisor, HKSC; and S. Raju, cochair, HKSC.

Local IEEE Members, RPGs, and faculty members at the IEEE SSCS barbecue gathering.



This IEEE SSCS research seminar attracted participants to share and be inspired by research.

Hong Kong school students working toward a place in the winner's circle during the IEEE Electronic Endeavor Match circuit design competition.

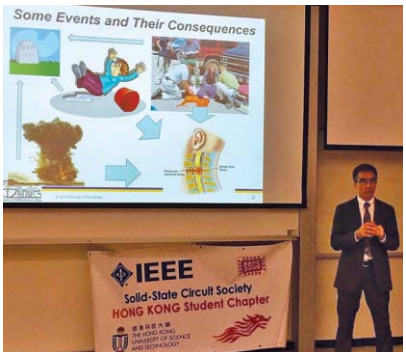
Hong Kong students during the practice session for the IEEE Electronic Endeavor Match.

IEEE Electronic Winter Camp children learning about circuit design.

IEEE Electronic Winter Camp children hard at work in their circuit design lab session.

the IEEE SSCS HKSC held an IEEE Electronic Endeavor Match for school children at Hong Kong Science Park on the 22 April 2017. The event included a practice session followed by a circuit design competition. Budding engineers attended the event, some of whom showed good problem-solving skills and initiative in their designs.

On 6 May 2017, the IEEE SSCS HKSC and the HKUST Electrical and Computer Engineering (ECE) Department hosted a barbecue gathering for local IEEE Members, research postgraduate students (RPGs), and faculty members. The event was organized to nurture friendships, increase interaction among RPGs and faculty members, and let people know about the Student Chapter and its activities in HKUST. Approximately 60 people attended the gathering.



Prof. Maysam Ghovanloo sharing his research on implantable and wearable microelectronic devices.

HKSC also organized a research seminar on 23 May 2017. Accepted conference papers were presented by students to share their research with others. The presentations were followed by healthy discussions and Q&A sessions. This research seminar proved to be very inspiring to the more than 15 RPGs in attendance.

The IEEE SSCS achieved its aim of connecting students with leading industry and academic pioneers, RPGs and ECE Department faculty members, as well as each other. It also inspired the next generation of potential engineers through its successful outreach programs.

—Khawaja Qasim Maqbool
Chair, IEEE SSCS Hong Kong Student Chapter

IEEE SSCS DL Pieter Harpe at SEMINATEC 2017

The 12th Workshop on Semiconductors and Micro & Nano Technology (SEMINATEC 2017) was held 27–28 April 2017 at the University of Sao Paulo (USP), Brazil. SEMINATEC 2017 was a continuation of 11 previous workshops, all focused on technology trends in the areas of micro- and nanotechnology. This year, SEMINATEC was organized by USP's Integrated Systems Laboratory and São Paulo State University (UNESP, the São João da Boa Vista campus). Support and funding was provided by the IEEE Electron Devices Society (EDS) Chapter, the EDS Student Chapter of the University of Campinas, the EDS Student Chapter of the Centro Universitário da FEI, the IEEE Solid-State Circuits Society (SSCS) Chapter of USP, the SSCS Student Chapter of USP, and the Brazilian Microelectronic Society (MTTS). The goal of this event was to promote interaction among industry, academics, research and development centers, and government and students, all looking for opportunities to improve their education, research, and technology.

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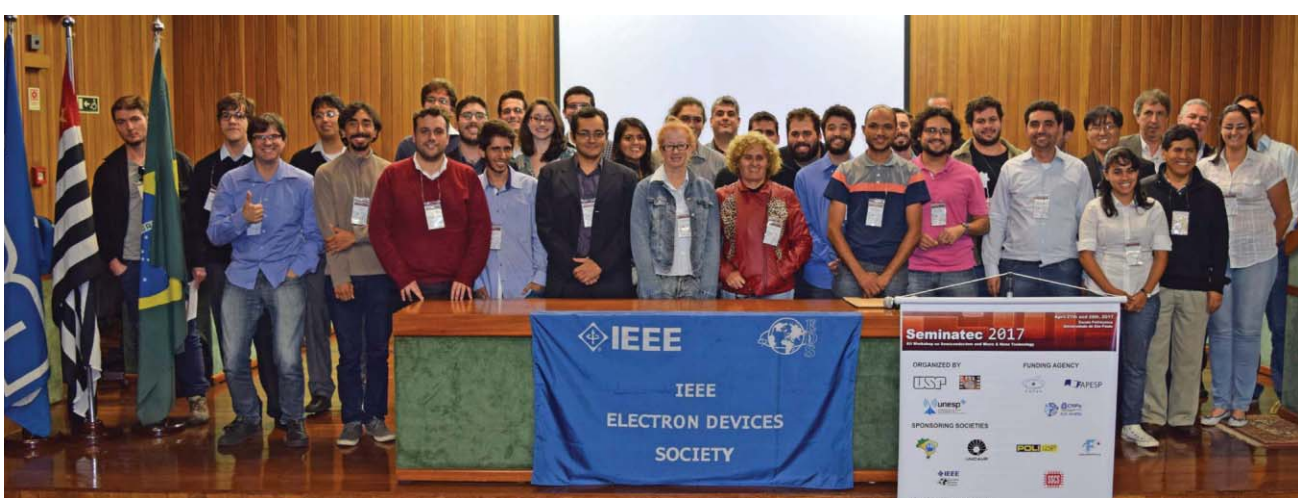
More than 120 participants from academia, research institutes, and industry attended SEMINATEC 2017. Such a relatively high attendance reflects the enormous success of the event's organization and indicates the substantial and growing interest over the years. This year, SEMINATEC's two-day intense program was centered around six overview lectures, one of them by an SSCS Distinguished Lecturer (DL), three by EDS DLs, one by an MTTS DL, and one from a research institution. The DLs and their talks were

- "Ultra Low-Power Analog Front-End Design" by Prof. Pieter Harpe, Eindhoven University of Technology, The Netherlands (SSCS DL)
- "Material and Device Challenges for the End of the Road Map CMOS Technologies" by Prof. Cor Claeys, KU Leuven and imec, Belgium (EDS DL)
- "Do Much with Very Little: Micropower Management for Energy Harvesting Application" by Enrico Sangiorgi, Bologna University, Italy (EDS DL)
- "Low Frequency Noise as a Diagnostic Tool in Advanced MOSFET Technologies" by Bogdan Cretu, CAEN University, France
- "NanoMEMS: Enabling the Internet of Things" by Hector J. De Los Santos, NanoMENS Research, California (MTTS DL)
- "FOSS TCAD/EDA Tools for Semiconductor Device Modeling" by Wladyslaw Grabinski, MOS-AK Association, Suisse (EDS DL).

Harpe gave two very interesting talks. The first lecture, on 26 April 2017, was "SAR ADCs for IoT: Basics and Innovations." In this seminar, Harpe provided an overview of the basics of successive approximation (SAR) analog-to-digital converters (ADCs) and introduced the latest architectural innovations that have led to unprecedented performance metrics. Even though SAR ADCs have been around for a very long time, they received a lot of attention recently, thanks to their power efficiency and beneficial scaling with technology. Harpe covered topics such as SAR ADC architectural issues, circuit design considerations,

SEMINATEC 2017 lecturers and organizing committee members. Front row (from left): Wilhelmus Van Noije, Paula Agopian, Enrico Sangiorgi, Cor Claeys, and Hector J. De Los Santos. Second row (from left): Pieter Harpe, Marcelo Pavanello, Newton Frateschi, José Diniz, Wladyslaw Grabenski, Bogdan Cretu, and General Chair João Antonio Martino.



The SEMINATEC 2017 poster presenters at USP, Brazil.

and algorithm levels. Advanced examples for the Internet of Things such as high-resolution SAR ADCs were presented.

Harpe gave a second talk, "Ultra Low-Power Analog Front-End Design" on 28 April 2017. He provided an overview on the design of a nanopower analog front-end including preamplification and analog-to-digital conversion. He discussed fundamentals on power efficiency in analog and mixed-signal circuits and presented considerations in terms of low-voltage operation and PVT reliability. Harpe also discussed one complete system implementation in more detail, including the amplifier, ADC, biasing stages, and clock generation. As an example, he presented very interesting experiment results on the design of an 3-nW signal acquisition IC integrating an amplifier with 2.1 NEF and a 1.5 fJ/conversion-step ADC, where first a system overview and optimization of amplifiers and 10-b SAR ADC designed in 65-nm CMOS were given, and then details on the measurements were presented and discussed.

In addition to the scientific lectures, five companies that supply equipment or services in the field of semiconductors were invited to give half-hour presentations describing their activities and needs for research and human resources to academia and industry in the region. To attract more students at the undergraduate, master's, and Ph.D. levels, a poster session was organized, where 51 selected technical papers were presented and discussed. During the closing session, the best paper award winners were announced in three categories: processing technology, devices, and design. More details are available at http://www.psi.poli.usp.br/seminatec2017/.

—Wilhelmus Van Noije
Chair, South Brazil Chapter
SSC

Why I'm an SSCS Member: Alice Wang

The IEEE Solid-State Circuits Society (SSCS) has almost 10,000 members worldwide. This new feature in the "People" column highlights the importance of Society membership and what it means to be a member of our Society. Tell us why you're an SSCS member; e-mail abira.sengupta@ieee.org to be featured.

What Is the Best Part of Being a Member of the IEEE SSCS?

The best part of being an SSCS member is attending conferences such as the International Solid-State Circuits Conference (ISSCC). It's a great network of people to meet, and all the experts are present at the conferences. It's an opportunity to learn about the latest research and what is going on in the field.

How Has SSCS Helped You Professionally?

I have been pretty involved in the ISSCC since graduate school. At that time, I was a young engineer, a new hire, and felt intimidated by all of the experts. ISSCC and SSCS are excellent platforms to exercise leadership skills and gain courage. At conferences like ISSCC, you will give a presentation in front of hundreds of people. The first time is really scary, but after conquering that, it gets easier to do public speaking. ISSCC and SSCS has helped me polish the skills needed to give high-quality presentations for work.

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Alice Wang

Tell Us About Your Work with the Women in Circuits Initiative

I am currently the chair of the SSCS Women in Circuits (WiC) Committee. Right now only 4% of the Society membership are women, which is very low compared to other Societies. We are working on organizing different networking events and helping women gain more confidence and leadership skills. We are really trying to engage women and show them that the Society can do a lot for their careers and SSCS membership can add a lot of value to their lives.

Why Is IEEE and SSCS Membership Important?

The IEEE works very hard to understand the trends of the semiconductor industry and where the industry is headed. It is important to know what the future holds, and the IEEE and SSCS help us understand this. The IEEE and SSCS add value to my career by giving me the necessary training, leadership skills, and networking opportunities. We are all in this community together.

Alice Wang

Alice Wang received her bachelor's, master's, and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, in 1997, 1998, and 2004, respectively. She wrote the paper "A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology" with Prof. Anantha Chandrakasan that inspired a new research field in ultra-low power technology. After receiving her Ph.D. degree, she spent eight years at Texas Instruments developing low-power circuit and system technology for mobile, application processors, and radios. Her work on low-power technology has been showcased in 30+ IEEE publications, and she has coauthored two books. She is a Senior Member of the IEEE. Currently, she is an assistant general manager in high-performance processor technology at MediaTek, working on advanced processors for consumer electronics including smartphones, tablets and smart TVs, and managing the foundation IP teams (standard cell library, memory, and input/output). She was elected to the SSCS Administrative Committee (2017–2019) and leads the WiC Committee.

—Abira Sengupta

In Step with Rabia Tugce Yazicigil

One of the SSCS's next generation of luminaries

Dr. Rabia Tugce Yazicigil, an IEEE Solid-State Circuits Society (SSCS) young professional member, is already on the path to make a positive impact on the Society. A budding leader and successful engineer, Rabia is part of the next generation of our Society's luminaries.

Rabia is currently a postdoctoral associate with the Electrical Engineering and Computer Science (EECS) Department at the Massachusetts Institute of Technology (MIT), working with Prof. Anantha P. Chandrakasan. Rabia received her B.S. degree from Sabanci University in 2009, and her M.S. degree from École Polytechnique Fédérale de Lausanne in 2011. Her master's thesis was advised by Prof. Christian Enz under Platform Circuit Technology Underlying Heterogeneous Nano and Tera Systems Program. Rabia received her Ph.D. degree in electrical engineering from Columbia University, New York, in 2016 under Prof. Peter R. Kinget and coadvised by Prof. John Wright.

This article is part of a series highlighting an SSCS member. If you would like to recommend a member to be featured or you would like to be highlighted, please e-mail News Editor Abira Sengupta (abira.sengupta@ieee.org.

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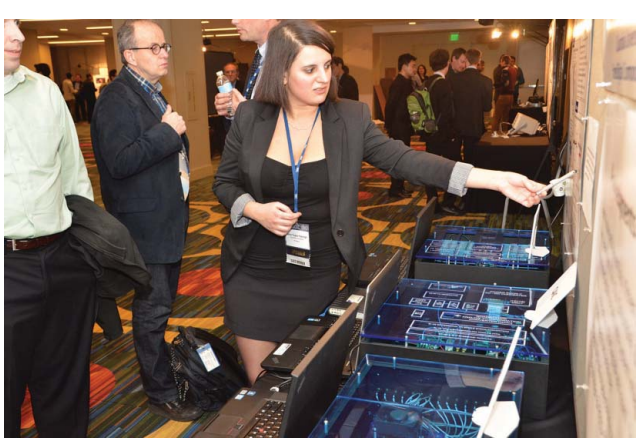
Rabia Tugce Yazicigil

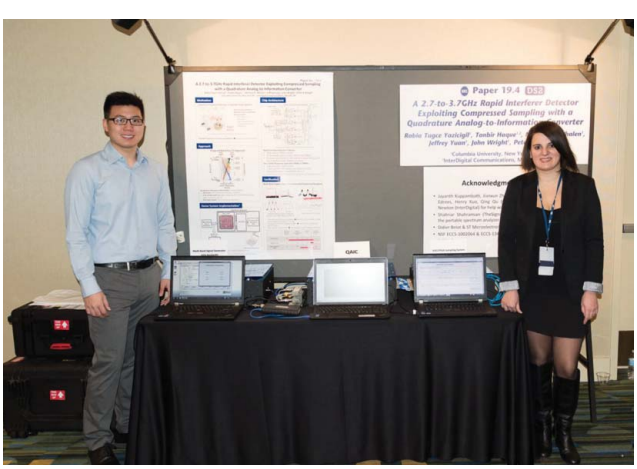
Rabia has received a number of awards highlighting her successes during her Ph.D. work: the 2016 Electrical Engineering Collaborative Research Award for her Ph.D. research on compressive sampling applications in rapid radio frequency (RF) spectrum sensing, second place at the 2015 Bell Labs Future X Days Student Research Competition, 2015 Analog Devices Inc. Outstanding Student Designer Award, and the 2014 Columbia University Millman Teaching Assistant Award.

One of Rabia's biggest career accomplishments was being selected to present her Ph.D. research work in the 2015 MIT Rising Stars in Electrical Engineering Computer Science. This annual workshop, created in 2012 by MIT EECS Department Head Chandrakasan, brings together the top women in EECS for two days of research presentations and informal panels. The program is aimed at women navigating the initial stages of their academic career. Because of her presentation and talk at this workshop, Rabia was invited to join MIT as a postdoctoral researcher to work with Chandrakasan.

Rabia's research interests include analog and RF ICs, energy-efficient wireless systems, novel digital signal processing algorithms, and secure wireless communications. She is currently working on ultra-low-power secure wireless communications for the Internet of Things applications at MIT. "Security is the most important consideration in future low-power wireless networks focused on connecting edge devices. It has been shown that life-critical implantable devices controlled over a wireless link can now be attacked, motivating the need to establish end-to-end secure system solutions," Rabia said. She is codeveloping



At ISSCC 2015, Rabia presented her first paper on her Ph.D. research. The compressed-sensing rapid interferer detector system was also demonstrated at the ISSCC demo session in a live experiment.



Rabia and a senior undergraduate student she mentored at Columbia University at an ISSCC 2015 demo session.

The SSCS workshop Recent Advances in Analog Circuit Design was organized by Rabia in 2016. The invited speakers and workshop organizers (from left): Anantha P. Chandrakasan, Willy Sansen, Peter R. Kinget, Gabriele Manganaro, Rabia Tugce Yazicigil, and Bruce Hecht.

Rabia came in second place at the Bell Labs Future X Days Student Research Competition in 2015.

wireless protocols and secure RF radio architectures that provide unique security in physical layer to enable new security paradigms for the next generation of wireless connectivity. Recently, Daniel Richman, the undergraduate student Rabia was mentoring this year on the ultra-low-power secure wireless protocol research, received the 2017 SuperUROP Outstanding Research Project Award from the MIT EECS Department.

Rabia has been an SSCS member since she was a graduate student. She became involved with the Women in Circuits (WiC) Committee in 2016. The goal of the committee is to increase female recruitment, retention, and advancement within the SSCS. Rabia has been an integral part of many WiC Committee events, including the International Solid-State Circuits (ISSCC) 2017 networking luncheon and the upcoming new ISSCC 2018 WiC Workshop. Rabia is also an active member of the SSCS Boston Chapter, where she has organized various events including distinguished lectures and mini-workshops. She was one of the organizers and speakers of the Spectrum Crunch?—RF Circuit and System Innovations to Tackle the Spectrum Scanning Challenge workshop at IEEE European Solid-State Circuits Conference (ESSCIRC) 2016, coorganized by Dr. Jan Craninckx and Prof. Peter Kinget.

Rabia and fellow participants of the 2015 MIT Rising Stars in Electrical Engineering Computer Science. In the center right next to Rabia is the late professor emerita Mildred Dresselhaus, known as the "queen of carbon science."

Rabia dancing the tango at Columbia University.

FUN FACTS ABOUT RABIA

- Rabia has been dancing the tango since she was an undergraduate student. She still dances the tango every week at MIT.
- Rabia has been trained as a swimmer since she was a child, and it's one of her favorite hobbies.

Rabia credits SSCS with influencing her life by shaping her personal development. "Being an active member of SSCS and organizing events through the SSCS Boston Chapter and the WiC has helped improve my leadership skills," she said. She also said that SSCS membership has had a profound impact on her career and professional development.

"It's a rewarding experience to be part of the SSCS community. The Society makes it possible to meet the experts in the field of ICs and helps you build a professional network," Rabia said. "As a young professional, I believe that these connections can open doors for future collaboration and provide professional support for years to come."

—Abira Sengupta

SSCS Treasurer Wanda Gass Engages the Future Generation of Female Engineers

In 2013, 47% of students taking high school physics were female, but only 31% of the AP physics exam takers were female. In 2014, women earned fewer than one in five of the bachelor's degrees awarded in engineering, computing, and physics. In the United States, only 18% of engineering students are women. To battle these statistics, Wanda Gass, IEEE Solid-State Circuits Society (SSCS) treasurer, created Design Connect Create.

Design Connect Create is a two-week day camp that strives to prepare young women for their first physics class in high school. The objectives of the program are to increase young women's academic performance in science, technology, engineering, and mathematics (STEM) courses, increase the number of women pursuing a STEM major in college, and expand their passion for the challenges and rewards of a STEM career. In addition to teaching various physics and math concepts, the summer camp helps young women prepare for the challenge of STEM courses, exposes them to role models and career opportunities, and emphasizes the importance of physics, engineering, and math.

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Experiments with liquid nitrogen.

A camp attendee rides on a hovercraft.

Design Connect Create is a two-week day camp that strives to prepare young women for their first physics class in high school.

Sound wave nodes illustrated using a Chandi plate.

Camp attendees learn about the properties of optics using a concave mirror.

The idea for the camp came from a group called High-Tech High Heels, which partnered with Texas Instruments to fund the program in 2003. The program has been offered in the Dallas school district every summer since then.

"The idea to replicate the camp so that more girls could be served by the program led to the creation of Design Connect Create in 2014," said Gass. The number of young women who have participated in the camp has grown from 71 students in 2014 to 177 in 2016. In 2017, Design Connect Create offered eight camp sessions in several cities in Texas with an estimated attendance of more than 250 young women.

Camp activities include:

- a magical demonstration of the principle of inertia
- exploring the properties of static electricity
- engineering design challenges
- reverse engineering a circuit topography
- visiting a high-tech company and meeting the summer interns
- riding on a hovercraft
- matching the motion graph
- charting your path through a maze
- calculating the collision point of toy cars
- using liquid nitrogen to make ice cream.

Design Connect Create camp alumna Lisbet Tudon speaks highly of her experience at the camp. "I've had the opportunity to attend this wonderful camp. It was a great experience and helped me develop my career goals," Tudon said. "I am a currently a senior in high school and attended the camp the summer before my junior year. I took pre-AP physics and am currently taking AP physics. Because of my interest in engineering, I applied for and was awarded the Texas Tech Presidential Scholarship (along with several other engineering scholarships), and I know that Design Connect Create helped contribute to my success. I will be attending Texas Tech as a freshman engineering student this fall," she said.

If you'd like to learn more about Design Connect Create, visit www.designconnectcreate.org.

—Abira Sengupta

SSC

Society Leaders and Industry Luminaries Speak About Opportunities and Challenges in the IC Industry

The young professionals (YPs) and student members of the IEEE Solid-State Circuits Society (SSCS) enjoyed food, drink, and friendly conversation at a mentoring event organized by SSCS YP Chair Emre Ayranci at the IEEE Custom Integrated Circuits Conference (CICC) 2017 on 2 May 2017. This year's event attracted a large number of YPs and students.

Ayranci kicked off the event with a welcome and presentation about the numerous benefits of SSCS membership. The event featured two guest speakers and industry luminaries: Tyson Tuttle, chief executive officer (CEO) of Silicon Labs, Austin, Texas, and Daniel Cooley, senior vice president and general manager, Internet of Things Products, Silicon Labs, Austin, Texas. Tuttle and Cooley spoke of their journeys and experiences. Both offered advice to the future generation of the Society and the field.

Tuttle gave six solid pieces of advice:

1) Pay attention to the business. Understand finance and return on investment. Understand the market, the market trends, and, most importantly, the competition. It is important to innovate on something that matters and to have a business case.
2) If you're going to have a successful business, make sure you invest properly. You will have to figure out how to sustain a business in both the short and long haul.
3) Don't pick a battle you can't win. When picking a team, or joining a company, make sure you pick a team that will win and be successful. Make sure you have the right talent.
4) Finish what you start. There is no greater feeling than starting the product, finishing the development, seeing it through production, and then seeing it used in products and sold.
5) Don't be afraid to move from one group to another. Don't be afraid to branch out.
6) Take a sociology class. Whether you become a manager, a CEO, or a professor, you will have to work in teams. It is important to understand people and have the ability to see things through other people's eyes. You must be able to motivate people as well.

Cooley gave three pieces of practical advice:

1) You have to find your mentors as they will not come to you. The best mentors will like being a mentor. Find those people, find those relationships and make a list of questions. Read the paper, "How to be a Star Engineer." There are many sociological and psychological tips in the paper, which is an integral part of your career.
2) You'll have multiple careers in your lifetime. You will start doing one thing and then migrate into another. You should actively seek out new opportunities. You don't want to get stale in what you're doing. Don't be afraid to go back to the basics. You may have to relearn certain things and have to keep your mind open.
3) Think ahead. You have to be thinking ahead the entire time. You have to think of what trends will drive the industry and understand these trends. It is easy since everyone is publishing on the Internet. Check out Twitter, check out Facebook, but be sure to attend conferences as well to learn about upcoming trends.

The attendees were engaged and enjoyed listening to both speakers.

It was a full house at the YPs Mentoring event at CICC.

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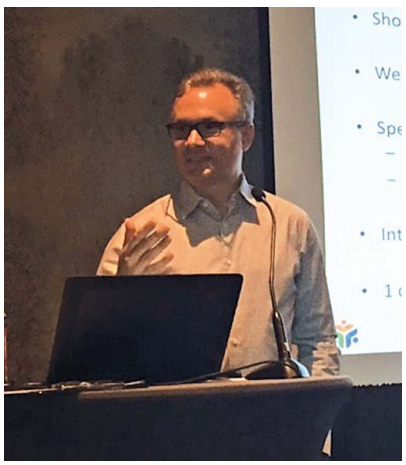

Tyson Tuttle speaks about opportunities and challenges faced in the IC industry.

Daniel Cooley offers three pieces of advice for students and young professionals.

"Having the chance to speak to a group of young professionals was energizing and inspiring. They are the next generation of engineers who will innovate and drive our industry, and we owe it to ourselves to do everything we can to encourage their development," said Cooley

Tuttle said, "The Young Professionals event at CICC in Austin was a great opportunity to speak with students and young engineers about the opportunities and challenges we face in the industry."

When the two speakers concluded, SSCS leaders, Administrative Committee members, Chapter chairs, and Distinguished Lecturers—who acted as the mentors—went around the room and described their journey to the field of ICs and how being an SSCS member has benefited them, helped them make valuable connections, and how their experiences with SSCS helped shape them. The YPs and mentors mingled and broke out into groups.

Ayranci said the event was meaningful to both the mentees and mentors, "Participants were very pleased to have the opportunity to learn from the experiences of our mentors and have a chance to talk one on one on a personal level and ask questions in such an intimate setup."

—Abira Sengupta

SSC

CIRCUIT INTUITIONS

(continued from p. 8)

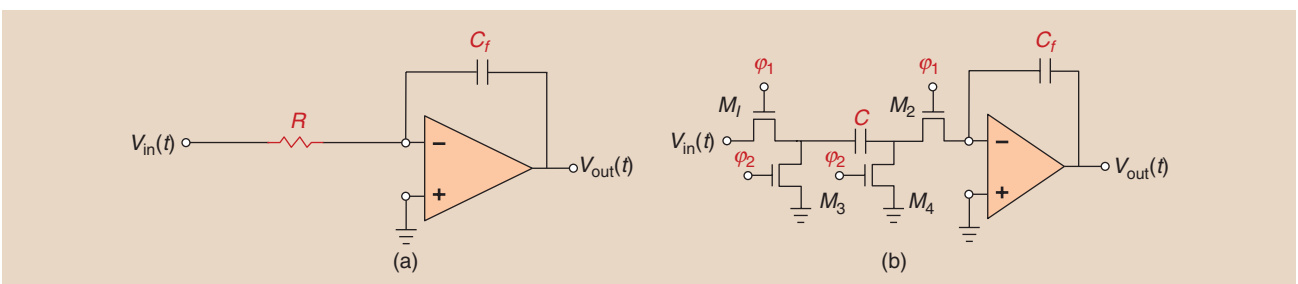

FIGURE 5: (a) An integrator using a resistor and a capacitor and (b) an integrator replacing the resistor with a parasitic-insensitive switched capacitor.

provide a voltage at the output. In other words, we can write

$$v_{out}(t) = -\frac{1}{RC_f}\int_0^t v_{in}(t)\,dt. \qquad (5)$$

In the switched-capacitor version of this integrator, shown in Figure 5(b), we simply replace the resistor with its parasitic-insensitive switched-capacitor equivalent. Accordingly, we can write a new expression for $v_{out}(t)$:

$$v_{out}(t) = \frac{-1}{T}\frac{C}{C_f}\int_0^t v_{in}(t)\,dt. \qquad (6)$$

A comparison between (5) and (6) reveals one of the most desirable features of the switched capacitor circuits: while the multiplying factor in (5) is the product of R and C, which may have as much as a 10% variation in an IC fabrication process, the corresponding factor in (6) is a ratio of two capacitances, which has a variation within 0.1%.

I end this article with an observation and a question for the readers. There appears to be a discrepancy between the expression for the equivalent resistance in (4) of this column and (2) of Maxwell's book, as shown in Figure 1. Can you explain this discrepancy?

In summary, if we view a resistor as an element that transfers charge from one terminal to another at a constant rate, we can implement it using a capacitor and two switches, as shown in Figure 2, where we transfer an average charge $C(V_1 - V_2)$ per period, effectively mimicking the behavior of a resistor whose resistance is T/C. This implementation forms the basis of a class of circuits known as switched-capacitor circuits.

Reference

[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. London, U.K.: Oxford Univ. Press, 2014.

SSC

Highlights of CICC 2017

The 38th annual IEEE Custom Integrated Circuits Conference (CICC 2017) was held 30 April to 3 May 2017 in Austin, the heart of the Texas hill country, for the first time. The conference, sponsored by the IEEE Solid-State Circuits Society (SSCS), enjoyed the support of the local IC design engineering community and a good level of worldwide participation.

The conference officially opened on Monday, 1 May, with a keynote presentation from Dr. Hans Stork, senior vice president and chief technology officer of ON Semiconductor, focusing on the key engineering requirements and tradeoffs that the semiconductor industry is facing in the enablement of the autonomously moving devices that will become part of our daily life in the next decade.

This year, the Education Sessions were scheduled on the Sunday (30 April) preceding the technical sessions to minimize possible attendance conflicts with regular papers presentations. Admission to these sessions was included with the regular conference registration, making them a great addition for the conference participant to get educated on advanced topics like mm-wave, time-domain, FD-SOI, and deep submicron Fin-FET design, as well as a refresh on fundamental topics of precision analog and mixed-signal design, like filters, data converter, phase-locked loops, and power converters. In addition, there was one special tutorial focusing on diversity and addressing how to leverage the strengths of female engineers in today's business environment. Educational sessions will be soon available online for SSCS members. The exact dates and the portal will be communicated via the SSCS e-newsletter and website.

Starting this year, the conference focus was steered more toward solid-state circuit design, including general analog design techniques, power management, data converters, wireless and radio frequency systems, wireline communication systems, as well as emerging technologies. The technical sessions also included design foundations presentations on the areas of computer-aided design, manufacturing, and measurement and testing, with the aim to provide important tutorial material to the circuit design community. Wireless papers covered advanced topics on 5G and mm-wave, focusing on massive multi-input, multi-output and energy efficiency.

The Wireline session had a rich agenda on serializer/deserializer and optical communication circuits, with many focused on PAM-4. Analog techniques papers included high-precision and ultra-low-power circuits design, extreme low-jitter clocking techniques, while the power management session covered both linear regulators and dc-dc devices, including switched capacitor converters. The data converter session presented several advanced techniques on successive approximation (SAR) and time-to-digital converters, and hybrid oversampling techniques including SAR and voltage-controlled oscillator-based converters in the noise-shaping loop. Many of the papers were based on advanced technologies like FinFET and FD-SOI.

The Emerging Technologies sessions covered several topics like advanced NVM (ReRAM), biomedical circuits, security circuits (PUF, non-cloneable functions, and random number generation) and nontraditional computing (neural networks, neuromorphic circuits, and machine learning). In particular, one of the emerging sessions covered multidisciplinary applications of electronic circuits: flexible substrates, energy harvesting sensors on power lines, and optically assisted high-bandwidth electronics.

The technical presentations were complemented by three Forum sessions and three Panel sessions. The Forums offered invited presentations focusing on "hot" IC topics that are currently receiving extensive research efforts and support, including emerging design techniques for data convertors (a traditionally strong topic at CICC), self-sustaining Internet of Things intersecting low-power electronics/radios with new power management techniques and energy-harvesting, as well as 5G circuits and systems, which is currently a major research focus in wireless electronics experiencing an explosive growth. The panels fostered vibrant and even controversial discussions on emerging topics that may greatly impact the IC field in the near future. Hardware and software security and bioinspired learning and inference systems, both of which are at the crossroads of circuit hardware, system architectures, and software designs, where covered by two of the panels. A third panel session had a more educational focus, and the panelists showcased their retrospectives on favorite analog/mixed-signal circuits that are often used as interesting interview questions.

Stimulating social happenings like the Monday evening welcome reception,

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RAMESH HARIJANI

Pavan Kumar Hanumolu presents at one of the CICC sessions.

RAMESH HARIJANI

Behind the scenes at CICC 2017.

RAMESH HARIJANI

SSCS President Jan Van der Spiegel talks about SSCS member benefits at the CICC plenary session.

RAMESH HARIJANI

The plenary session.

RAMESH HARIJANI

Dr. Hans Stork delivered the keynote at CICC 2017.

RAMESH HARIJANI

Session 6 at CICC 2017.

RAMESH HARJANI

CICC attendees mingled at the CICC Luncheon held on Tuesday, 2 May.

RAMESH HARJANI

Dr. Christopher Mangelsdorf presents at the CICC 2017 Luncheon.

RAMESH HARJANI

Attendees listening intently to Dr. Christopher Mangelsdorf's talk at the CICC 2017 luncheon.

RAMESH HARJANI

Tyson Tuttle, CEO of Silicon Labs, gives young professionals and students advice at the CICC 2017 Young Professionals Mentoring Event.

the Tuesday evening conference reception, and conference luncheon were a nice contrast to the technical character of CICC and provided additional opportunities for discussion and peer networking in a relaxed environment. The conference luncheon featured Dr. Christopher Mangelsdorf, fellow at Analog Devices, who offered a very entertaining but sharp and visionary presentation on the "struggle" of analog designers through 50 years of Moore's law. As always, the CICC luncheon was one of the main attractions of the conference. The luncheon was sold out during preregistration.

This year, CICC also included a well-attended mentoring session for young professionals in industry and academia, sponsored by the SSCS. Mentors included SSCS executives and leaders, various members of the Technical Program Committee, invited speakers, and special guests. An article on the mentoring session can be found in the "Society News" column of this issue.

In addition, a new Ph.D. student sponsorship initiative program to attract more student attendees and future student paper authors was established. The program was aimed at all first- and second-year Ph.D. students worldwide who have not previously attended CICC. A total of seven Ph.D. students were selected for the 2017 program, and sponsorship was provided to support their attendance at CICC 2017.

CICC 2017 wouldn't have been possible without the generous support received by the IEEE, SSCS, and 12 corporate and academic sponsors. A particular thank you goes to Silicon Labs (platinum level), the general conference and proceedings sponsor, and Analog Devices (gold level) for support for the Best Regular Paper Award and for Internet access during the conference.

The 39th annual edition of the conference (CICC 2018) is currently in the planning stages and will be held in San Diego, California. CICC 2019 is scheduled to return to Austin. The plan for future editions is to expand to cities such as Boston and Chicago.

—Alessandro Piovaccari
Ramesh Harjani
Hua Wang
Kimo Tan
Don Thelen
SSC

CEDA Currents

The following is reprinted from *CEDA Currents*, May 2017 issue, a publication of the IEEE Council on Electronic Design Automation (CEDA). Please send contributions to Jose L. Ayala (jayala@fdi.ucm.es).

Code Ocean Is Live: Upload Your Algorithms

Code Ocean is a cloud-based executable research platform that allows authors to share their algorithms in an effort to make the world's scientific code more open and reproducible. Uploading your algorithms and associated data files to the Code Ocean site is easy. Anyone can run an algorithm posted to Code Ocean, modify it, and test the modifications. The published algorithm that an author posts will remain unchanged.

Any author that has had an IEEE journal article published on IEEE *Xplore* in the last five years can upload associated algorithms to Code Ocean by visiting https://codeocean.com/ieee/signup. Once the algorithm is uploaded to Code Ocean, it will automatically be linked to the associated article in IEEE *Xplore*. Users in IEEE *Xplore* will be able to discover and access the link to run the algorithm in Code Ocean.

For more information, please check: https://www.ieee.org/documents/code_ocean_feb_2017.pdf.

1st IEEE CEDA IoT Student Challenge Sponsored by Texas Instruments

On 27 March, and during the conference DATE, it took place the first edition of the IoT Student challenge, cosponsored by IEEE CEDA and Texas Instruments (TI). During that exciting day, 20 teams had the opportunity to practice with TI's SimpleLink Technology. Each participant received a Launchpad and a Sensortag that allowed them to set up their own wireless sensor network during the tutorial as well as later on at home. The new CC1350 dual-band technology allows cost-effective, ultra-low-power, 2.4-GHz and sub-1 GHz IoT applications. The combination of easy mobile phone integration with long-range connectivity including a 32-b ARM Cortex-M3 processor on a single chip, and the varied flow of data from ten different types of sensors gave the students the opportunity to innovate in a broad range of personal or academic projects.

Peter Spevak (from TI) provided the training and conducted the challenge, while IEEE CEDA's president (Shishpal Rawat) and Dominique Poissonnier (from TI) awarded the four winners of the challenge during the DATE reception.

OpenDesign Flow Database

In recent years, there have been a slew of design automation contests and released benchmarks. ISPD place&route contests, DAC placement contests, timing analysis contests at TAU, and CAD contests at ICCAD are good examples in the past, and more of new contests are planned in upcoming conferences. Nevertheless, most contests focus only on the point tool problems and fail in addressing the design flow or cooptimization among design tools.

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IEEE Embedded Systems Letters is open for submissions. Visit mc.manuscriptcentral.com/les-ieee.

IEEE Design & Test is open for submissions. Visit mc.manuscriptcentral.com/dandt and ieee-ceda.org/publications/d-t/paper-submission.

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UPCOMING CONFERENCES (YAO-WEN CHANG, YWCHANG@NTU.EDU.TW)

- GLSVLSI
  Alberta, Canada
  10–12 May 2017
- WIE ILC
  San Jose, California
  22–23 May 2017
- ETS
  Limassol, Cyprus
  22–26 May 2017
- DAC
  Austin, Texas
  18–22 June 2017

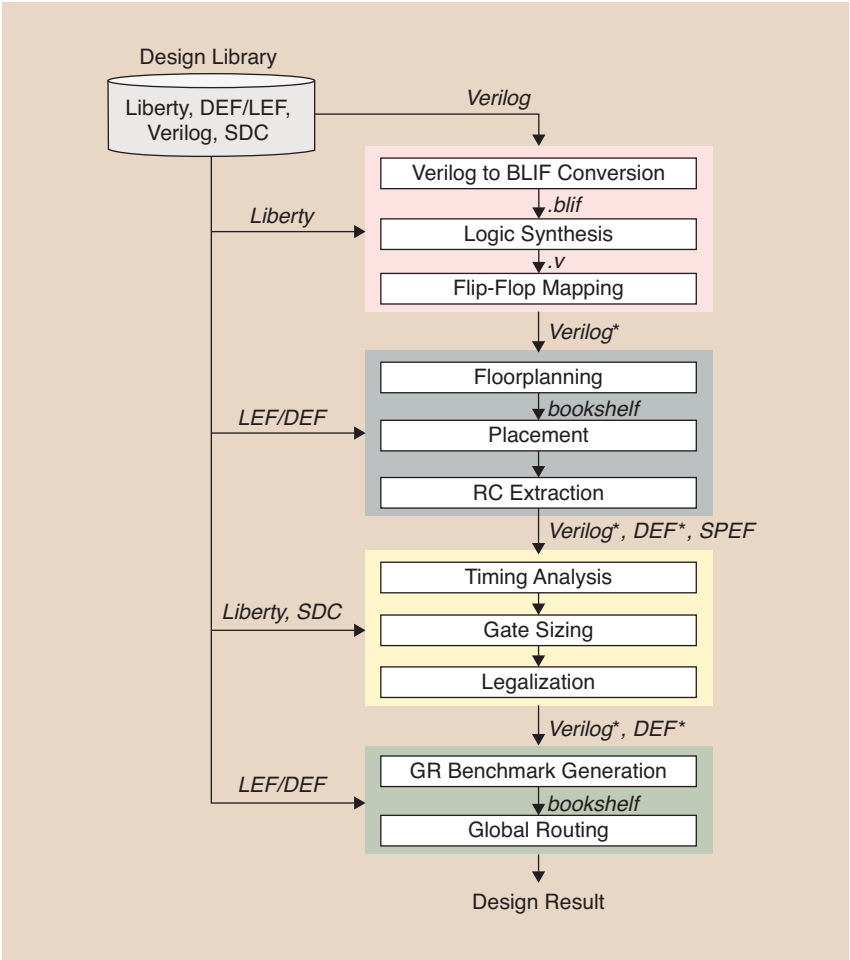

FIGURE 1

IEEE CEDA Design Automation Technical Committee (DATC) develops OpenDesign Flow Database to direct attention to the overall design flow from logic design to physical synthesis. The goals are to provide 1) an academic reference design flow purely composed by past CAD contest results, 2) the database for design benchmarks and point tool libraries, and 3) standard design input/output formats to build a customized design flow by composing point tool libraries. Figure 1 illustrates the overview of OpenDesign Flow Database. It includes public academic binaries for logic synthesis, placement, timing analysis, gate sizing, and global routing, as well as additional translation scripts that enable data exchange between tools. The reference flow will be expanded to include more academic point tools in the near future. If you are interested in providing tools, please kindly contact us.

Papers in *IEEE Embedded Systems Letters*

The top-five accessed articles from *IEEE Embedded Systems Letters* in February 2017 were as follows:

- "A Compact Portable Microwave Life-Detection Device for Finding Survivors," by F. JalaliBidgoli et al.
- "Arduino Debugger," by J. Dolinay et al.
- "Public Key Authentication and Key Agreement in IoT Devices With Minimal Airtime Consumption," by S. Sciancalepore et al.
- "Energy Efficient Outdoor Light Monitoring and Control Architecture Using Embedded System," by Z. Kaleem, T.M. Yoon, and C. Lee
- "Partitioning Real-Time Tasks With Replications on Multiprocessor Embedded Systems," by J. Deny Lin, A.M.K. Cheng, and G. Gercek.

Papers in *IEEE Design and Test*

The top-five accessed articles from *IEEE Design and Test* in February 2017 were as follows:

- "Exploring Exploration: A Tutorial Introduction to Embedded Systems Design Space Exploration," by A. Pimentel
- "High-Bandwidth Memory (HBM) Test Challenges and Solutions," by Hongshin Jun et al.
- "Approximate Computing: A Survey," by Q. Xu, T. Mytkowicz, and N.S. Kim
- "Unleashing Fury: A New Paradigm for 3-D Design and Test," by M. Alfano et al.
- "Automotive Cyber–Physical Systems: A Tutorial Introduction," by S. Chakraborty et al.

SSC

CONFERENCE CALENDAR

SSCS-SPONSORED CONFERENCES

2017

43rd IEEE European Solid-State Circuits Conference (ESSCIRC 2017)
http://www.esscirc-essderc2017.org/
11–14 September
Leuven, Belgium
Paper due date: passed

Asian Solid-State Circuits Conference (A-SSCC)
http://www.a-sscc2017.org/
6–8 November
Seoul, Korea
Paper due date: passed

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2018

2018 IEEE International Solid-State Circuits Conference (ISSCC)
http://isscc.org/
11–15 February
San Francisco, California, USA
Paper due date: TBD

2018 IEEE Symposium on VLSI Circuits
http://www.vlsisymposium.org/
19–22 June
Hawaii, USA
Paper due date: TBD

SSCS TECHNICALLY COSPONSORED CONFERENCES

2017

2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)
http://biocas2017.org/
11–14 September
Torino, Italy
Paper due date: passed
Demonstration proposal date: passed

IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)
http://ieee-bctm.org/
19–21 October
Miami, Florida, USA
Call for papers: passed

2018

2018 IEEE Symposium on VLSI Technology
http://vlsisymposium.org/
19–21 June
Location TBD
Paper due date: TBD

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